SECTION 1
HOW TO USE THIS MANUAL

CONTENTS

INTRODUCTION

WARNING

SERVICING DESCRIBED IN THIS MANUAL IS TO BE PERFORMED BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK OR DAMAGE TO THE INSTRUMENT, PERFORM ONLY THE SERVICING EXPLICITLY DESCRIBED IN THIS MANUAL.

The Helios I Service Manual is a service and maintenance guide (including replacement parts lists) to the Computer Front End. The Service Manual complements the Helios I System Manual, which provides installation, operating, and system configuration information.

The Service Manual covers standard mainframe and option assemblies, and provides general maintenance, cleaning, performance testing, calibration, and board-level troubleshooting procedures. The Helios I Service Manual is to be used by technicians and maintenance personnel who need detailed, technical information about the electronics of the Front End.

Information needed to maintain the Front End and to isolate problems to circuit board level is given in this manual. Theories of operation and schematics for the mainframe and options are provided to aid those qualified to troubleshoot beyond the circuit board level.

When the defective assembly has been identified, returning the Front End to service can frequently be expedited by using our Module Exchange Program (MEP). Because MEP cannot be performed in some countries, we recommend that you contact your local Fluke authorized Service Facility (listed in Appendix C) to obtain instructions for replacement or repair.

ORGANIZATION

Section 1 How to Use This Manual

Describes the organization and use of the Service Manual.

Section 2 Gene al Information

Describes the Front End and its available accessories and options. Required test equipment, shipping, and factory service information are included here.

Section 3 Theory of Operation

Covers the theory of operation for the Front End mainframe. Option assembly theory is contained in the individual option subsections of Sections 8 and 9.

Section 4 Maintenance

General maintenance of the instrument, cleaning instructions and procedures to gain access to and remove mainframe assemblies are included here.

Section 5 Testing and Troubleshooting

Consists of mainframe performance tests and troubleshooting procedures designed to isolate a malfunction to the circuit board level. Component level troubleshooting may be performed using the Theory of Operation (Section 3) and Schematic Diagrams (Section 7).

Section 6 List of Replaceable Parts

Contains parts lists for the Front End mainframe and gives parts ordering information. Option assembly parts lists are in the individual subsections of Sections 8 and 9.

Section 7 Schematic Diagrams

Presents Front End mainframe schematics on foldout pages. Schematics for option assemblies are located in the individual option subsections.

Section 8 Options -160 Through -169

Covers Options -160 through -169 in subsections ordered numerically by option number. Includes theory of operation, performance test procedures, calibration instructions (where applicable), schematics, and a replacement parts list.

Section 9 Options -170 Through -179

Covers Options -170 through -179 in subsections ordered numerically by option number. Includes theory of operation, performance test procedures, calibration instructions (where applicable), schematics, and a replacement parts list.

Section 9A Scan/Alarm Option -201

Includes description, theory of operation, performance test procedure, parts list, and schematic diagram.

Section 10 Appendices

A Specifications
B Federal Supply Codes for Manufacturers
C Service Centers
D Manual Status Information

HOW TO USE THE MANUAL SET

The Helios I Computer Front End is supported by a manual set consisting of two manuals.

System Manual

The Helios I Computer Front End System Manual describes all aspects of Helios I installation and operation.

The System Manual provides all the information necessary to define required functions, identify system requirements, make the necessary hardware connections, and verify correct operation. An inexperienced user may need all this information to install the Front End and make it operational. A user who is already familiar with the instrument may only need to refer to this information occasionally. In either case, each element of the installation process is easily accessible and fully referenced.

Service Manual

The Helios I Computer Front End Service Manual is the maintenance guide to the Front End.

The Service Manual contains general maintenance, cleaning, performance testing, calibration, and board-level troubleshooting procedures. The Service Manual also includes theory of operation, parts lists, and schematic diagrams for mainframe and option assemblies.

CONVENTIONS

- Reference to the Instrument

  The Helios I Computer Front End will generally be referred to as the "Front End". The terms "Helios I" or "Computer Front End" will also be used. Where a Helios I or Computer Front End equipped with a Scan/Alarm (-201) option is concerned, the term "(Scan/Alarm)" is attached to the instrument name.

- Printed Circuit Assembly

  A printed circuit assembly (pca) is a printed circuit board with components mounted on it.

- Logic Polarity of Signals

  Logic signals whose names are followed by "(L)" are asserted or active low. On the schematic the same signal can be represented as "SIGNAL(L)" or SIGNAL overscored by a vinculum.

  When a signal is followed by "(H)" or has no parenthetical postscript, it is active or asserted high.

- Address Notations

  Hexadecimal representation of memory addresses takes the form

  0x0000

  Memory addresses ranges, where specified, are inclusive.

  For example, address range

  0x0000 to 0x2000

  includes addresses "0000" and "2000".

- Keystroke Notations

  The following conventions are used to identify syntax keystrokes and differentiate them from surrounding text:

  (xxx) When associated with a keyword, a lower-case word in parentheses indicates an input required by the user.

  For example, the command

  DEF CHAN(channel[s]) = DCIN <CR>

  means that the user must specify "channel[s]" to be defined as direct current input channel[s] to have a valid command.

  XXX Indicates a literal keyword to be entered by the user.

  For example,

  TIME

  means that you enter the literal word "TIME" or "time".

  The Front End is case insensitive and will accept any combination of upper- or lower-case letters. However, all Front End keywords in this manual which are not part of actual computer programs will appear in upper-case letters to distinguish them from surrounding text.

  <XXX> Angle brackets around all upper-case letters means press the <XXX> key.

  For example,

  <CR>

  means press CARRIAGE RETURN, RETURN, or ENTER (according to your keyboard.

.. "Double Periods" designate an inclusive range.

For example,

```
CHAN(0..99) = 1 <CR>
```

assigns logic "1" to channels 0 through 99.

SECTION 2
GENERAL INFORMATION

CONTENTS

DESCRIPTION

The Fluke Helios I Computer Front End is a highly accurate, easy-to-use data acquisition and control subsystem that can be used with any kind of personal or mainframe computer.

The Computer Front End is a medium speed, smart intermediary between a computer and a real world measurement application. With capacity ranging from a single channel in a minimal configuration to 1500 channels in a fully expanded system (1000 channels if the Scan/Alarm option is installed), the Front End can be adapted to a wide array of applications.

The Front End gathers data and generates control or stimulus signals through a standard computer interface. It combines a full range of measurement capabilities and is easy to program. The Front End's chassis includes:

- An RS-232-C and an RS-422 standard serial interface port for communication with a host computer. (Serial printer port available with Scan/Alarm option.)
- A microcomputer with ROM and RAM to provide local intelligence.
- Six option slots that accept any of a range of measurement and control modules. This family of options supports a variety of both analog and digital inputs and outputs.

  Expansion chassis can be added to accommodate more input/output channels, up to a maximum of 1500 (standard system) or 1000 (Scan/Alarm option system).

Power Requirements

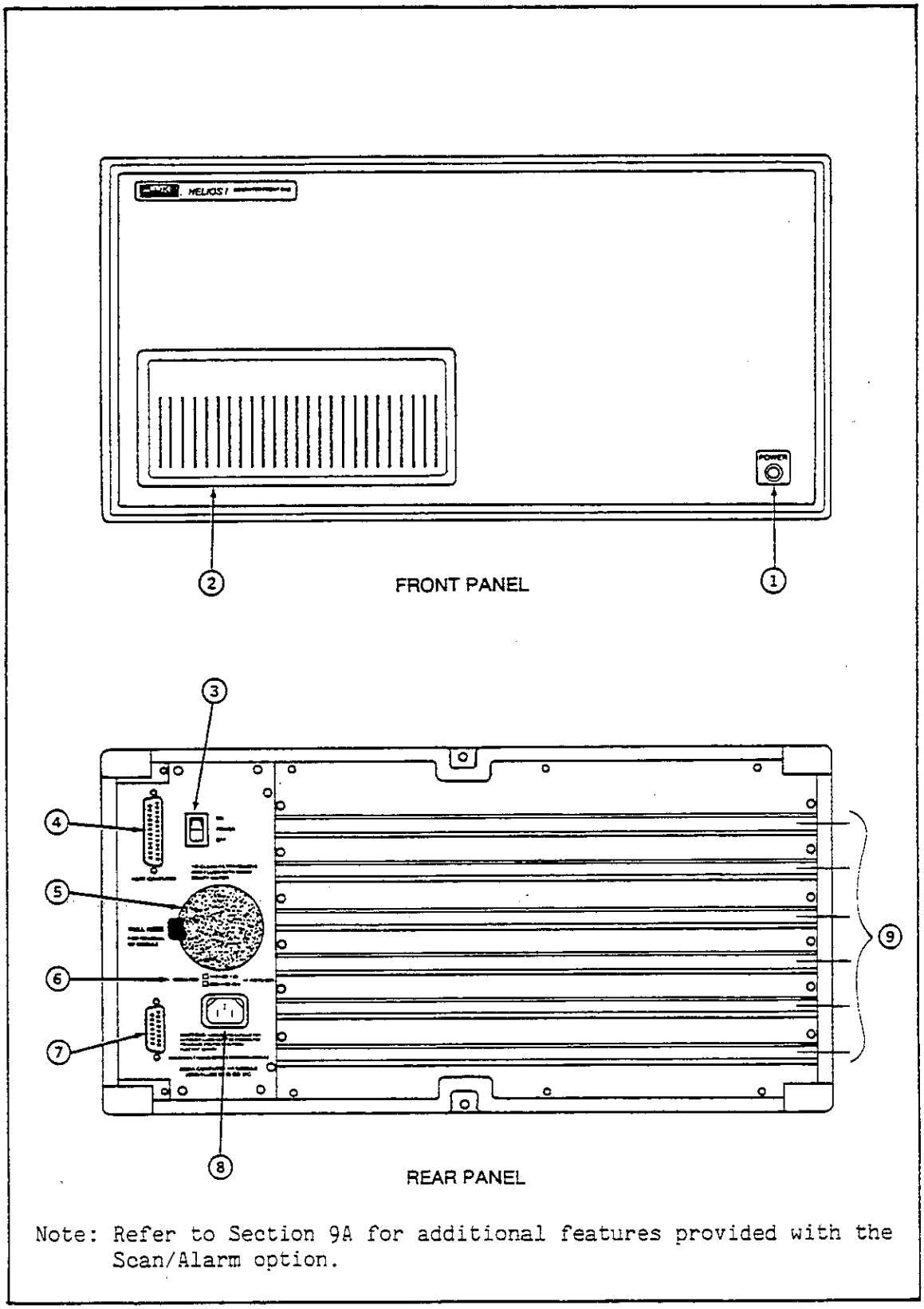
The Front End operates on either of two ac line voltage ranges: 90 to 132V ac, or 180 to 264V ac. Line frequency for either range may be from 47 through 440 Hz. If you need to verify or change either setting, refer to Section 4 for details.

CAUTION

Incorrect voltage selection may damage the Computer Interface Module and void your warranty. If the voltage is not set for the correct operating voltage, the unit will either fail to operate, or will be severely damaged.

External Features and Connectors

The features and connectors located on the front and rear panels of the Front End are shown in Figure 2-1 and described Table 2-1. Six horizontal slots are available for installing scanners, A/D Converters, and other measurement and control options.



Note: Refer to Section 9A for additional features provided with the Scan/Alarm option.

Figure 2-1. Front and Rear Panels

Table 2-1. Front and Rear Panel Features

ITEM	FEATURE	DESCRIPTION
1	Power Indicator	Green LED. Lit when Power is ON
2	Grill	Ventilation Grill
3	Switch	ON/OFF Switch for ac Line Power
4	25-Pin Connector	RS-232-C/RS-422 Connector to Host
5	Filter	Washable, Removable Fan Filter
6	Voltage/Frequency	Silk Screened Annotation of Line Voltage Selection and Frequency
7	15-Pin Connector	Connector to 2281 Extension Chassis
8	AC Input	Standard Three-Prong Socket
9	Slots	Six Slots for Front End Options

Note: Refer to Section 9A for additional features provided with the Scan/Alarm option.

The Front End's external dimensions are shown in Figure 2-2.

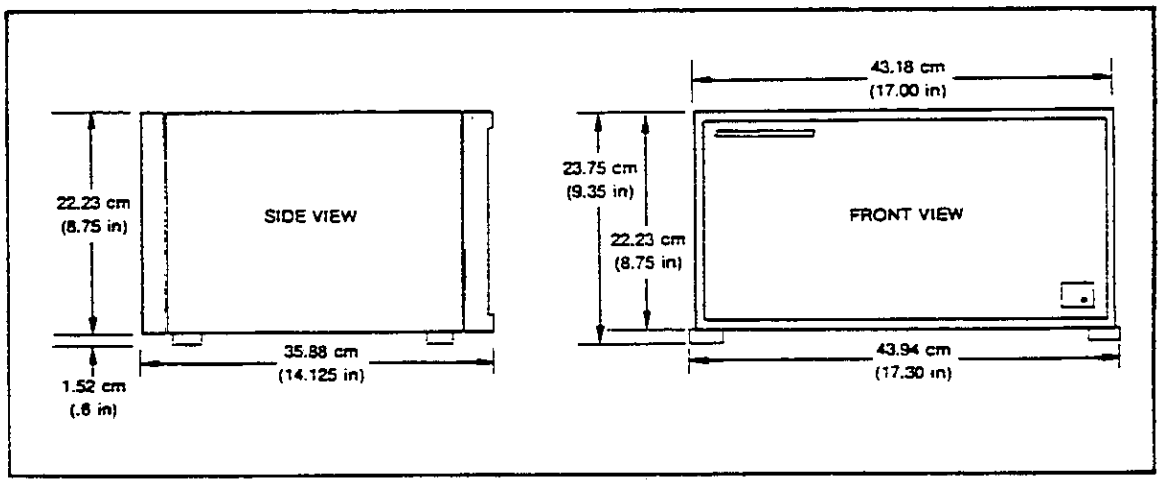


Figure 2-2. External Dimensions

REQUIRED TEST EQUIPMENT

Equipment required for all Front End performance tests and calibration procedures is listed in Table 2-2. Equipment required for each test is also listed with the procedure in the applicable section or subsection.

Table 2-2. Summary of Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
DC Calibrator	+31.3 mV +/- 20 uV +2.048V +/- 50 uV -2.048V +/- 2 uV of +2.048 500 mV +/- 20 uV 6.2V +/- 155 uV 6.8V +/- 0.1V 5.0V +/- 100 uV 7.9V +/- 200 uV 63V +/- 800 uV 1.008V +/- 40 uV	Fluke Model 343
Digital Multimeter DMM	Capable of measuring +12V dc	Fluke 77 or equivalent
Power Supply	Capable of sourcing +12V dc	Appropriate lab type
100:1 Divider	+/- 0.005%	Fluke Accessory Y2022
DC Voltmeter	+10V +/- 0.06V 50.0 mV +/- 0.001 mV 500.0 mV +/- 0.005 mV	Fluke Model 8502A
Resistance Calibrator	NA	Fluke 8505A
Resistor (4 each)	100 ohm 0.01% 5ppm/°C	Fluke Part No. 491720
Resistor (2 each)	100 ohm 0.1%	Fluke Part No. 357400

Table 2-2. Summary of Required Test Equipment (cont)

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Resistor	499 ohms 1% MF	Fluke Part No. 289256
Resistor, 2 each	220 ohms, 1W	Fluke Part No. 109462
Resistor	1 kilohm +/- 5%, 1/2W	Fluke Part No. 108597
Resistor	10 kilohm +/- 5%, 1/2W	Fluke Part No. 109165
Resistor	8 ohm +/- 0.25%, 1/2W	Fluke Part No. 641449
Oil or Water Bath	NA	
Mercury Thermometer	0.02 °C resolution	Princo ASTM-56C
Calibration Extender/Fixture	NA	Fluke Accessory Fluke Part No. 648741 (no substitute)
Digital Extender Assembly	NA	2400A-4021 Fluke Part No. 486910
Toggle Switch	Single-pole, double-throw	Fluke Part No. 493825

OPTIONS, ACCESSORIES, AND OTHER RELATED EQUIPMENT

All options available for the Front End at the time of this printing are listed in Table 2-3. Refer to Sections 8 and 9 of this manual for further information on options.

All accessories are listed in Table 2-4.

Table 2-5 lists other related equipment for use with the Front End.

Table 2-3. Options

NUMBER	NAME	FUNCTION
-160	AC Voltage Input Connector	AC to dc conversion, voltage division, screw-terminal connections (for use with -162).
-161	High Performance A/D A/D Converter	Analog-to-digital converter, dual slope integration.
-162	Thermocouple/DC Volts Scanner	Scans 20 channels, 1 microvolt, 3 poles/channel (for use with Options -160, -161, -171, -175, or -176).
-163	RTD/Resistance Scanner	Scans 20 channels, 4 poles per channel, 1 pole/decade, precision current source excitation (for use with Options -161, -177).
-164	Transducer Excitation Module	Contains one precision 2V or 4V source and five precision 1 mA current sources (for use with Options -162, -174, -175, -176 and 10 dc channels of -160).
-167	Counter/Totalizer	Measures frequency or counts events on six channels.
-168	Digital I/O Assembly	Provides 20 single-bit channels for alarm or status input or output or for BCD or binary input (for use with -169 or -179).
-169	Status Output Connector	Provides 20 screw-terminal connections for external digital devices (for use with -168).

Table 2-3. Options (cont)

NUMBER	NAME	FUNCTION
-170	Analog Output Assembly	Four-channel current (4 to 20 mA) or voltage (0V to 10V or -5V to +5V) outputs, 12 bits.
-171	Current Input Connector	Provides 20 current input connections each with a shunt resistor (for use with -162).
-174	Transducer Excitation Connector	Provides screw-terminal connections for voltage and current sources (for use with -164).
-175	Isothermal Input Connector	Provides screw-terminal connections for 20 thermocouple input channels (for use with -162).
-176	Voltage Input Connector	Provides screw-terminal connections for 20 voltage input scanner channels (for use with -162).
-177	RTD/Resistance Input Connector	Provides screw-terminal connections for 20 channels of 3- or 4-wire RTD or resistance measurement (for use with -163).
-179	Digital/Status Input Connector	Provides screw-terminal connections for binary or status digital input signals (for use with -168).
-201	Scan/Alarm	Provides automatic channel scanning with local printout and alarm annunciation. Replaces standard Computer Interface Module.

Table 2-4. Accessories

ACCESSORY	DESCRIPTION
Y2044 Rack Slide Kit	Slide kit for mounting the Front End or the 2281A Extender Chassis in a 19-inch-wide, 24-inch-deep equipment rack.
Y2045 Rack Mount Kit	Mounting flanges for installing the Front End or the 2281A Extender Chassis in a 19-inch-wide, 24-inch-deep equipment rack.
Y2047 Extender Chassis Multi-Connector	Interconnection unit for connecting multiple 2281A Extender Chassis to the Front End.
Y2055 Serial Link Multi-Connector	Three-way connector assembly used in a multipoint serial link network
Digital Extender PCA Fluke Part No. 486910	Allows the Computer Interface Module to be extended out from the mainframe for troubleshooting.
Calibration Extender/ Fixture Fluke part No. 648741	Allows the horizontal pcas to be extended out from the mainframe for calibration or troubleshooting.

Table 2-5. Other Related Equipment

ITEM	DESCRIPTION
Fluke Model 2281A Extender Chassis	Allows adding extra channels by housing additional option assemblies.
Fluke 2281A-402 Extender Chassis Cable	Cable to connect a Front End to a 2281A Extender Chassis or to link two 2281A Extender Chassis. Ordered in lengths from 1 to 1000 meters.
Fluke 2281A-403 Connectors for Extender Chassis Cable	Connectors for each end of a 2281A-402 Cable. Installed onto the cable at the factory.
Fluke 2281A-431 Power Supply for the 2281A Extender Chassis	Optional power supply for the 2281A Extender Chassis. Used for remote operation in some cases.
Fluke Accessories Y1702, Y1703 and Y1705 Null Modem Cables	Used to direct connect the Front End with the host computer. Three lengths
Fluke Accessories Y1707 and Y1708 RS-232-C Cables	Used to connect the Front End to another RS-232-C device. Two lengths.

SHIPPING INFORMATION

When you receive the instrument, inspect the shipping container for any possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If it is necessary to reship the instrument, use the original container. If the original container is not available, a new one can be obtained from the John Fluke Manufacturing Co., Inc. upon request.

SERVICE INFORMATION

The Front End is warranted for a period of one year upon delivery to the original purchaser. The warranty is located, in the front of this manual, after the title page.

Factory calibration and service for each Fluke product is available at various locations worldwide. A complete list of these service centers is given in Section 10 of this manual. If requested, an estimate will be provided to the customer before any work is begun on an instrument whose warranty period has expired.

Maintenance plans are available to maintain the Front End at your site, to supplement the normal warranty period, or to do both. For specific information, contact your nearest Fluke Technical Service Center or Sales Representative.

SECTION 3
THEORY OF OPERATION

CONTENTS

INTRODUCTION

Section 3 provides the theory of operation for the Helios I Computer Front End mainframe. The theory of operation is complemented by block diagrams, simplified schematics, and tables, which aid in clarifying concepts. Schematic diagrams for the Motherboard and Computer Interface Assembly are in Section 7. When unfolded, a schematic diagram remains fully visible while the manual is open to any preceding page. This arrangement is useful when simultaneously reading the theory of operation and viewing related areas of the schematic diagram.

Section 3 covers only the theory of operation. Installation, operating, and configuration instructions for the Front End are located in the Helios I System Manual.

The Scan/Alarm Option (-201) uses a different Computer Interface Module than described in this section. Refer to Section 9A for the related theory of operation. All the other following theory in Section 3 applies to both versions of the Front End (with or without Scan/Alarm option).

Many optional modules and connectors are available. These provide the Front End with specific measurement and control functions. Theory of operation and a schematic diagram for each optional assembly and connector are provided in the subsection of Section 8 or Section 9 devoted to that option.

OVERALL FUNCTIONAL DESCRIPTION

To help clarify the relationship of the Front End's major functional blocks, refer to Figure 3-1 (a simplified block diagram of the Front End) while reading the overall functional description.

Blocks that are drawn in dashed lines represent optional assemblies; these assemblies are not required. However, any useful system will contain at least one data acquisition or control option, hereafter collectively referred to as serial link devices. These options can include, for example, the a/d converter, digital I/O, and analog I/O.

The serial link allows the CPU of the Front End mainframe to communicate with all measurement and control options in the system. The serial link can be extended outside the Front End Chassis to an Extender Chassis that also contains serial link device options. To communicate with the optional assemblies, the serial link uses RS-422 signals that are sent and received through two pairs of conductors. Through one pair, the computer interface transmits while the options listen. Through the other pair, the selected option can transmit only to the computer interface.

The following summary breaks down the Front End into its three major circuit blocks and briefly describes the function of each. The circuit analysis explains in detail how each of these three blocks operates.

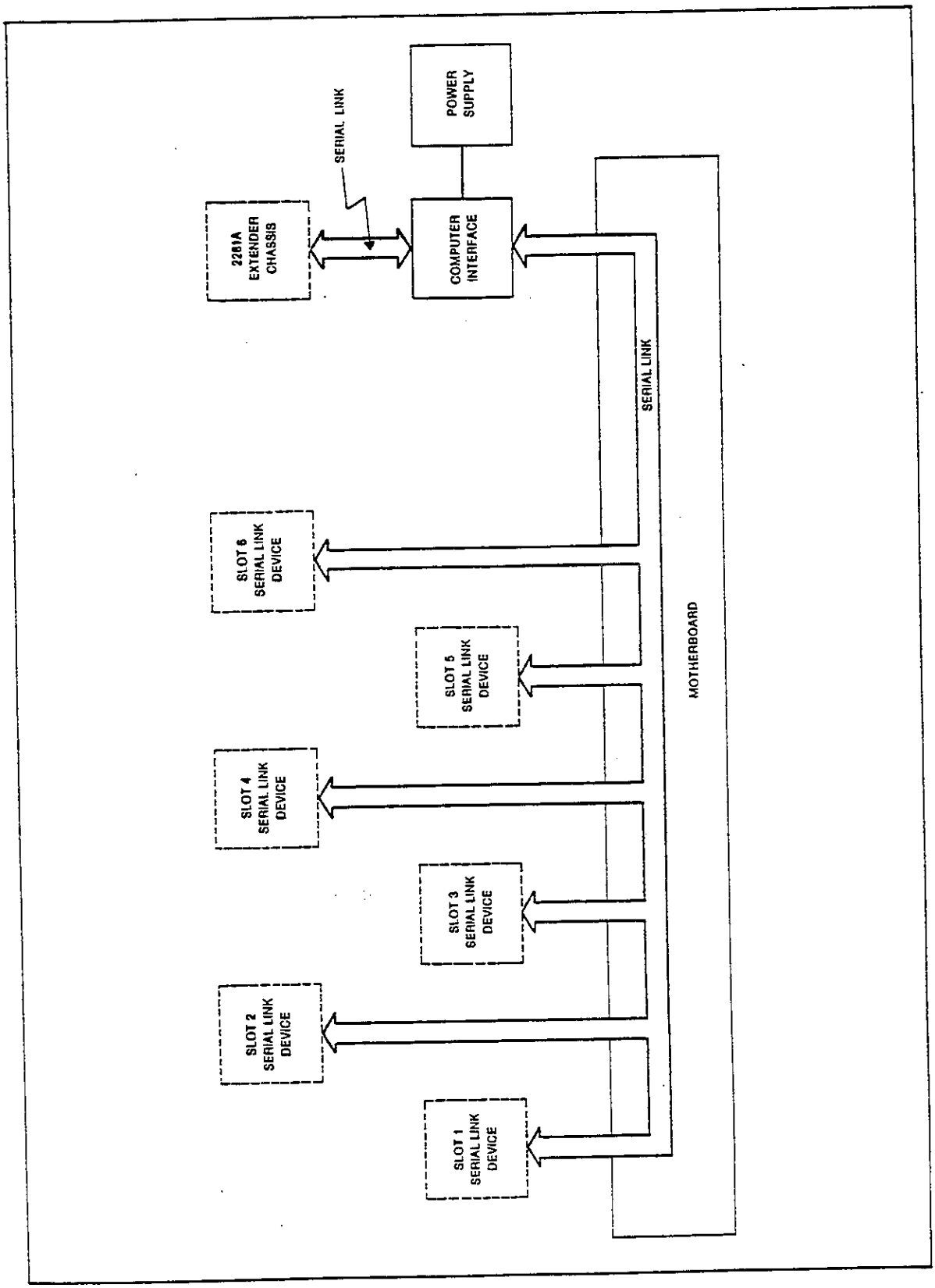


Figure 3-1. Mainframe Assemblies Block Diagram

- Chassis Motherboard

  The chassis Motherboard provides the interconnection between the Computer Interface Assembly and the serial link devices. It also, provides interconnection between A/D options and scanner options that are associated with the A/D.

- Computer Interface Assembly

  At the heart of the Front End is the Computer Interface Assembly. The Computer Interface Assembly is centered on the TMS-9995 microprocessor. This assembly provides the interface between the host computer and the measurement and control options. Commands from the host computer are interpreted and the appropriate responses are executed by the Computer Interface Assembly.

- Power Supply

  The power supply converts ac power into three regulated dc output voltages that provide power for all assemblies within the Front End and for serial link options installed in an Extender Chassis. The number of serial link options that can receive power from the mainframe power supply is limited. Further information on supplying power to these options is contained in Section 3, "Installation and Setup," of the Helios I Computer Front End System Manual.

More complete discussions of each of these major circuit blocks follow.

CHASSIS MOTHERBOARD

The Motherboard interconnects the Computer Interface Assembly and the serial link devices installed in the mainframe or extender chassis.

PCA card-edge connectors are mounted on one side of the Motherboard. Since the Motherboard PCA is designed to be used in other instruments, there are several places (not used by the Front End) where additional connectors can be mounted.

The schematic diagram for the Motherboard (see Section 7) contains information about all card-edge connectors that can be installed on the Motherboard. Therefore, the schematic shows several signal names that can be ignored. Connector J12 is used for connection to the Computer Interface Assembly and is labeled on the schematic as power supply. The only connections on J12 which are used are: RX+ (43), RX- (41), TX+ (44), TX- (42), GND1 (17, 18, 19, 20), GND3 (25, 26, 27, 28) and +24 (22,23).

Although the +24V line is used to supply power to the serial link devices, the Front End power supply actually supplies 12V. The serial link devices will operate off 10 to 25V.

COMPUTER INTERFACE ASSEMBLY

Figure 3-2 is a functional block diagram of the Computer Interface Assembly. This assembly can be thought of as consisting of 15 functional circuit blocks.

The discussion of the Computer Interface assembly begins with a functional description of the assembly as a whole, followed by a more specific discussion of each of the 15 functional blocks.

The CPU, which controls operations on the Computer Interface Assembly, is a TMS-9995 microprocessor. The TMS-9995 interfaces with ROM and RAM in the conventional manner and with various I/O devices through a communications register unit (CRU) and the address lines.

At power-up, the reset circuit initializes various circuit elements and keeps the CPU from operating until the supply voltage is within operational limits. When reset is released, the CPU begins execution as directed by the ROM.

The CPU initializes the system based on: 1) configuration switch settings, 2) data which remains in the non-volatile RAM during the power-down state, and 3) information about serial link devices that are detected through the serial link communication interface.

After initialization is complete, the host communication interface is ready to accept commands from the host and pass them on to the CPU for interpretation and execution. Commands from the host can result in placing data into RAM, reading and returning data from RAM, setting or reading the clock data, or performing a measurement or control function on a serial link device.

A description of each of the 15 functional blocks which make-up the Computer Interface Assembly follows.

Power ON/OFF Reset Circuit

The power ON/OFF reset circuit monitors the +5V power supply and asserts RESET(L) when the voltage is below 4.6V. U16 is powered from the +5B supply, which is backed up by battery if the power is OFF. This allows RESET(L) to be actively asserted when power is OFF, and it is used by the memory chip selector block to ensure that the RAMs are de-selected while the power is below 4.6V.

R24 and R26 form a precision voltage divider off the +5V supply. The output of the voltage divider is compared by U16 (a dual-voltage comparator) to 1.23V, which is produced by R27 and VR2 (a band-gap reference diode). On power-up, when the +5V supply has reached 4.6V, U16 removes the common on pin 1 and lets C14 begin to charge through R28 to the +5V supply. When the voltage across C14 reaches 1.23V, U16

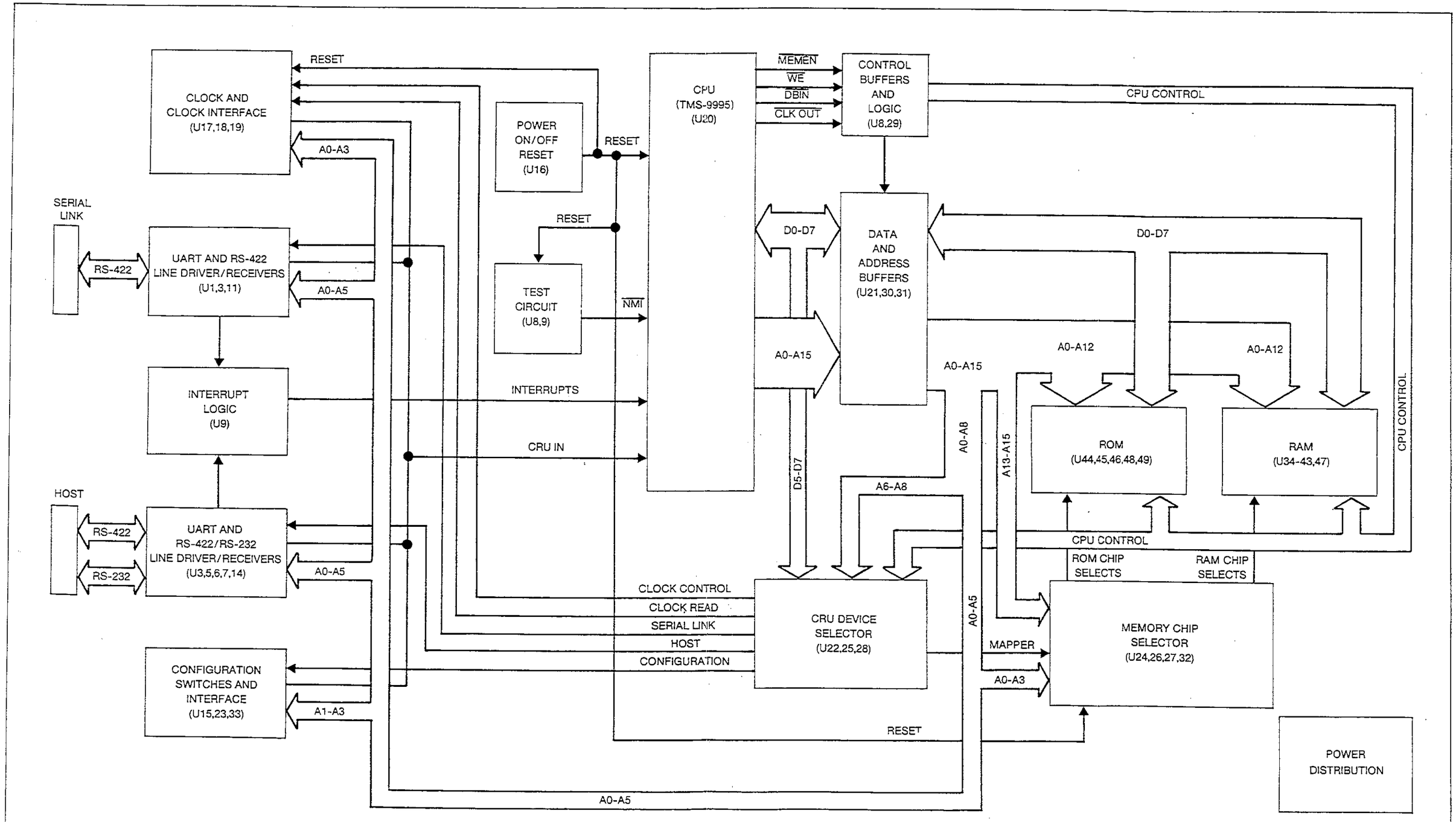


Figure 3-2. Computer Interface Assembly (Functional Block Diagram)

removes the common on pin 7, and RESET(L) is pulled to the +5V supply through R25. The time constant of C14 and R28 is short enough to ensure that the output pin 7 of U16 will transition without bounces and long enough to filter any bouncing that might occur when the first stage of U16 transitions.

Test Circuit

Part of U9 and U8 is used to form an R/S flip-flop, which can be used to stop and start CPU instruction execution.

The CPU is stopped by momentarily applying a low to pin 3 of J74, and it is started again by momentarily applying a low to pin 1 of J74.

Central Processor Unit (CPU)

The CPU is implemented by U20, a TMS-9995 16-bit microprocessor. The TMS-9995 onboard clock generator uses Y1, an 11.9808 MHz crystal, to determine the frequency of the clock. C18 and C19 are used to ensure proper capacitive loading for the onboard amplifiers.

Pull-up resistor, R32, de-asserts the HOLD(L) input on the TMS-9995 since this feature is not implemented.

Pull-up resistor, R33, asserts the READY input on the TMS-9995. When RESET(L) makes a low-to-high transition at power-on with READY asserted, the automatic first wait state generation feature of the TMS-9995 is selected. This causes one wait state to be added to every memory access cycle.

Data and Address Buffers

The 8-bit data bus is buffered by U30, an octal bus transceiver. The direction of data transfer is determined by the CPU control signal DBIN(L). This buffer, which is required due to the large number of memory ICs used in the Front End, is enabled only when DBIN(L) and MEMEN(L) are asserted.

The 16-bit address bus is buffered by octal buffers U21 and U31. These buffers are required due to the large number of memory ICs and CRU devices used in the Front End.

CPU Control Buffers and Logic

The CPU control signals MEMEN(L), WE(L)/CRUCLK(L), DBIN(L), and CLKOUT are buffered by U29, an octal buffer. This buffer is required due to the large number of memory ICs and CRU devices used in the Front End.

A buffered MEMEN(L) from U29, pin 9 is used on U30, pin 19 to enable the data bus buffer.

One of the inverters of U8 is used to generate the complement of WE(L)/CRUCLK(L) as required by some of the CRU devices.

Communication Register Unit (CRU) Device Selector Circuit

Figure 3-3 shows a schematic diagram of the CRU device selector circuit block. This circuit detects a CRU device input or output cycle by the CPU and selects the device based on the address bits A6 through A8.

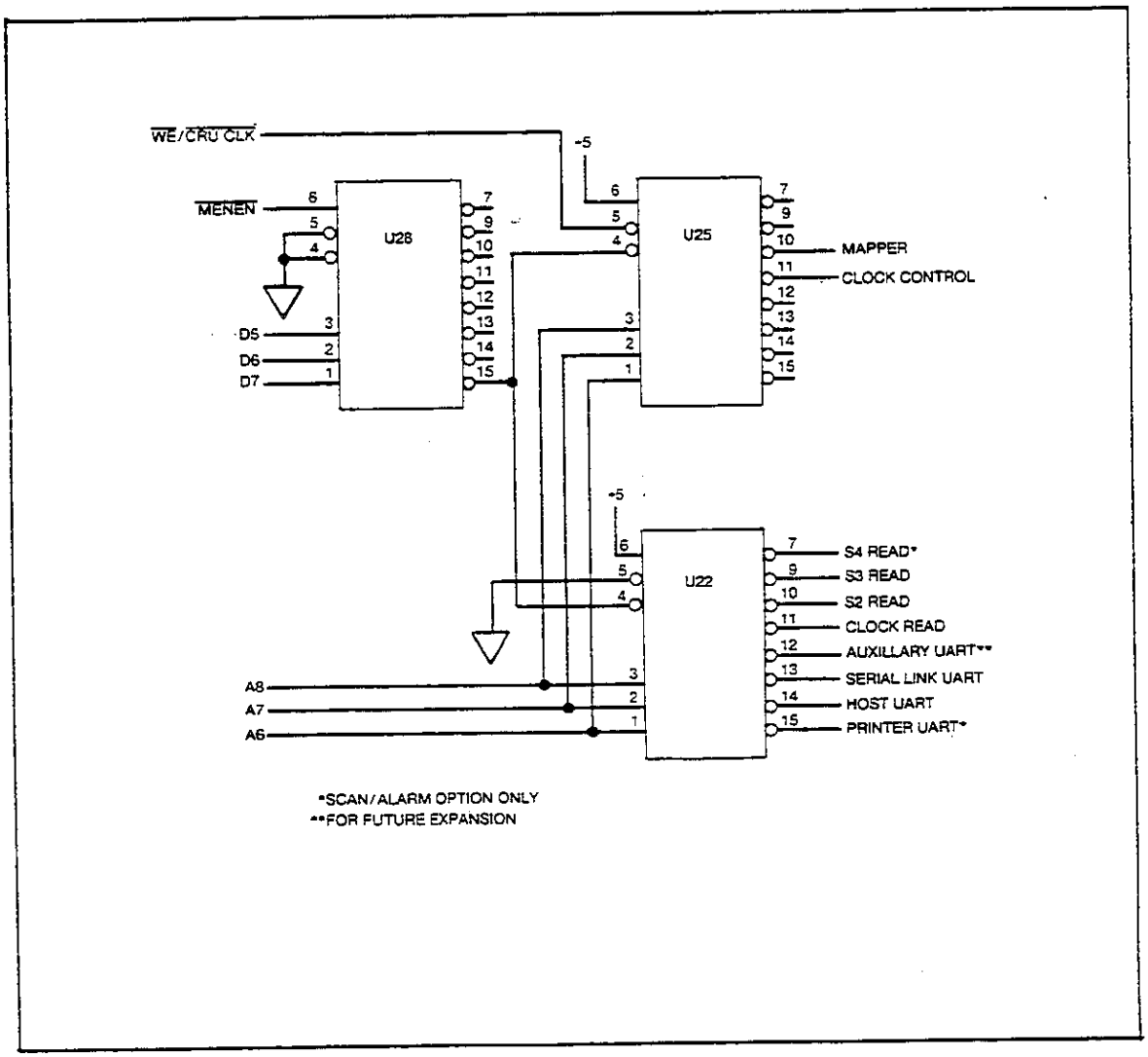


Figure 3-3. CRU Device Selector Circuit

When the data bits D5 through D7 are low and the control signal MEMEN(L) is high, U28 pin 15 will be low. Since the enable inputs on U22 pins 4, 5, and 6 are all asserted, the U22 output corresponding to the address bits A6 through A8 will be low. When the CRUCLK(L) control signal is low, all the enable inputs on U25 pins 4, 5, and 6 are asserted and the output corresponding to the address bits A6 through A8 will be low. In other words, when the CPU is requesting communication with a CRU device, one output of U22 will be low and one output of U25 will follow CRUCLK(L).

Table 3-1 shows the base address, the CRU device that is selected, and the type of transaction.

Table 3-1. CRU Device Selection

ADDRESS	INPUT	OUTPUT
0x0000	Printer Port	Printer Port
0x0040	Host Port	Host Port
0x0080	Serial Link	Serial Link
0x00C0	Auxiliary Port	Auxiliary Port
0x0100	Clock & Misc	Clock & Alarm
0x0140	Switch 2	Mapper & Misc
0x0180	Switch 3	Not Used
0x01C0	Switch 4	Not Used

Of the four ports that can be selected, the standard configuration Front End uses only the host and serial link ports. On the Scan/Alarm option (-201), switch 4 is used for the printer port.

The CRU device selector circuit can select multiple CRUs simultaneously. However, pins 10 and 11 on U22 enable CRU devices that are for input only, and pins 10 and 11 on U25 enable CRU devices that are for output only. When an output device is receiving data from the CPU and the CRUCLK(L) signal is toggling, the input-only device of the same address that is enabled by U22 will be inactive since DBIN(L) is high. When an input device is sending data to the CPU, the CRUCLK(L) signal is high and none of the outputs of U25 will be asserted.

Memory Chip Selector Circuit

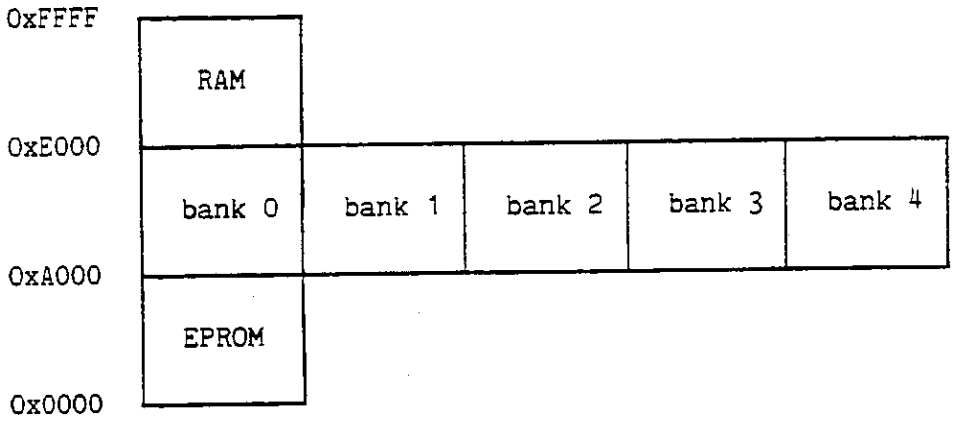
The memory chip selector circuit decodes the address bus and other inputs from the CPU via a CRU device to select one of 14 memory ICs for data transfer.

The CPU has the ability to address directly 64K bytes of memory with the 16-bit address bus. This address space contains EPROM (Erasable Programmable Read-Only Memory) and RAM (Random-Access Memory). Since the Front End requires more RAM for parameter and data storage than can be accommodated by this 64K-byte address space, part of the memory space is multiplied by using banks.

Figure 3-4 shows how the memory is organized.

U32, a 3-to-8 line decoder/multiplexer, asserts the output that corresponds to address bits A13 through A15 when the CPU control signal MEMEN(L) is asserted low.

Table 3-2 shows the relationship between the address bits and the chip that is selected.



NOTE: RAM bank 4 is not used by the Front End. It is available for future expansion.

Figure 3-4. Memory Organization

Table 3-2 Address Bits and Chip Selection

ADDRESS RANGE	U32 PIN ASSERTED	CHIP SELECTED
0x0000-0x1FFF	15	U46 (EPROM)
0x2000-0x3FFF	14	U49 (EPROM)
0x4000-0x5FFF	13	U45 (EPROM)
0x6000-0x7FFF	12	U48 (EPROM)
0x8000-0x9FFF	11	U44 (EPROM)
0xA000-0xBFFF	10	U27 (Bank selector)
0xC000-0xDFFF	9	U24 (Bank selector)
0xE000-0xFFFF	7	U47 (RAM)

When selected by U32, the 3-to-8 line decoder/multiplexers, U24 or U27 will assert the output that corresponds to the signals on the input pins 1, 2, and 3. These inputs are supplied as signals MM0 through MM2 from U26, an 8-bit addressable latch, which is used as a CRU output device. The CPU selects the proper bank for the data transaction and sets the bits into the appropriate outputs of U26 prior to accessing the RAM.

Table 3-3 shows the relationship between the mapper bits MM0 through MM2 and the RAM chip that is selected.

Table 3-3. Mapper Bits and RAM Chip Selection

MM2	MM1	MM0	U24 OR U27 PIN ASSERTED	RAM SELECTED IF U24 ENABLED	RAM SELECTED IF U27 ENABLED
0	0	0	15	U36	U38
0	0	1	14	U41	U43
0	1	0	13	U35	U37
0	1	1	12	U40	U42
1	0	0	11	U39	U34

U24 and U27 are CMOS ICs and have power applied from the +5B supply when Front End power is OFF. The enable input on pin 6 of U24 and U27 is connected to the power ON/OFF reset circuit. When the +5V supply is below 4.6V, the RESET(L) signal is asserted low, which de-selects U24 and U27, which in turn de-select all the banked RAMs. This ensures non-volatile memory retention of parameters and data. The inputs of U24 and U27 are pulled to the +5V supply by resistors in network Z6, since the drive signals originate from TTL-LS ICs.

Outputs on U26 pins 7 and 9 are made available for future expansion as additional mapper bits, and are not used by the Front End. Outputs on U26 pins 10, 11, and 12 are used to provide inputs from the CPU to the host communication interface circuitry.

The CPU sets the outputs of U26 with a CRU output cycle. The RESET(L) signal asserted at power up on U26 pin 15, CLEAR, causes all outputs to be set low. The address of the latch to be written to is from address bits A1 through A3, and the state of the latch is defined by address bit A0. The CRU device selector circuit supplies the enable input on U26 pin 14 as discussed above.

Read-Only Memory (ROM)

The Read-Only Memory that supplies the firmware for the CPU consists of five 8K-byte by 8-bit EPROMs (U44, U45, U46, U48, and U49).

The data in these EPROMs is retrieved by a CPU read cycle. Address bits A0 through A12 are decoded by each EPROM to determine the byte being fetched. The memory chip selector circuit discussed previously uses the remaining address bits A13 through A15 to provide the chip-select signal to pin 20 on one of the five EPROMs. The selected EPROM outputs data to the data bus when OE(L) is asserted low; OE(L) is the same as DBIN(L).

Capacitors C29, C30, C31, C38, and C39 are power supply bypass capacitors which reduce noise coupling through the power distribution circuit.

Wire jumpers W1, W2, W3, W5, and W6 are hardwired on the Computer Interface PCA as shown on the schematic diagram. These jumpers are provided for future modification and can be ignored.

Random-Access Memory (RAM)

The Random-Access Memory used by the CPU consists of nine 8K-byte by 8-bit CMOS static RAMs (U35 through U38, U40 through U43 and U47).

These RAMs are powered by the +5B (battery backed up) power supply so that the data is non-volatile when the power is OFF. The power ON/OFF reset circuit and the memory selector circuit ensure that the chip select input pin 20 is de-asserted high when the +5V supply is below 4.6V.

Data is written into these RAMs by a CPU write cycle. Address bits A0 through A12 are decoded by each RAM to determine the byte being written to. The memory chip selector circuit discussed previously uses the remaining address bits A13 through A15 and the memory mapper, U26, bits MM0 through MM2 to provide the chip select signal to pin 20 on one of the nine RAMs. The data on the data bus is written into the selected byte of the selected RAM when WE(L) is asserted low.

The data in these RAMs is retrieved by a CPU read cycle. Address bits A0 through A12 are decoded by each RAM to determine the byte being fetched. The memory chip selector circuit discussed previously uses the remaining address bits A13 through A15 and the memory mapper, U26, bits MM0 through MM2 to provide the chip select signal to pin 20 on one of the nine RAMs. The selected RAM outputs data to the data bus when OE(L) is asserted low: OE(L) is the same as DBIN(L).

Capacitors C22, C23, C25, C27, and C33 through C37 are power supply bypass capacitors which reduce noise coupling through the power distribution circuit.

Wire jumpers W4 and W7 on the Computer Interface PCA are as shown on the schematic diagram for the standard Computer Interface Assembly. Refer to Section 9A for Scan/Alarm option use of these jumpers.

Sockets for U34 and U39 and associated power supply bypass capacitors C21 and C32 are not used with the standard Computer Interface Assembly and can be ignored. Refer to Section 9A for Scan/Alarm option use of these components.

Configuration Switches and Interface Circuit

The circuit block containing the configuration switches and interface circuit consists of CRU devices and DIP switches for the input of configuration information to the CPU. There are three identical circuits in this block and each operates the same; however the data obtained is for different use by the CPU. Switch pack S2, pull-up resistor network Z1, and data selector/multiplexer U15 are used to provide information about the host computer communication port. Switch pack S3, pull-up resister network Z2, and data selector/multiplexer U23 are used to provide information about the host computer protocol and local line frequency. Switch pack S4, pull-up resistor network Z3, and data selector/multiplexer U33 are not used by the standard Computer Interface Assembly. They are used with the Scan/Alarm option, which is documented in Section 9A of this manual.

When the CRU device selector circuit detects that the CPU is accessing this circuit, the appropriate output of U22 asserts the strobe input, pin 7, of the data selector/multiplexer U15 or U23. Address bits A1 through A3 are used to address each switch that is connected with a pull-up resistor to each input of U15 or U23.

If the selected switch is closed, a low is output on pin 5 of the enabled data selector/multiplexer. If the selected switch is open, a high is output on pin 5 of the enabled data selector/multiplexer. These pin 5 outputs are the CRUIN signal for the CPU and will be input while DBIN(L) is asserted low.

The function of each switch is shown on the decal located on the rear bezel of the Front End.

This circuit is only used at power-up. Therefore, if the configuration is changed, the power to the Front End must be cycled for the CPU to be reconfigured.

Clock and Clock Interface Circuit

The clock and clock interface circuit provides the Front End with a non-volatile system clock and calendar. U19 is a CMOS calendar/clock IC that is powered from the +5B (battery backed up) power supply. Interface to the CPU is provided by CRU devices for control and reading of the clock.

The CRU device that allows the CPU to output control signals and data to U19, is U18, an 8-bit addressable latch. The CPU sets the outputs of U18 with a CRU output cycle. The RESET(L) signal asserted at power-up on U18 pin 15, CLEAR, causes all outputs to be set low. The address of the latch to be written to is from address bits A1 through A3 and the state of the latch is defined by address bit A0. The CRU device selector circuit supplies the enable input on U18 pin 14 as discussed above.

When the CRU device selector circuit detects that the CPU is accessing this circuit to read data, the output of U22 pin 11 is asserted low and provides the strobe input, pin 7, of U17, a data selector/multiplexer.

Table 3-4 defines the signals used for control and setting of U19.

Table 3-4. U19 Control Signals

CRU ADDRESS	U18 PIN	U19 PIN	SIGNAL
0x0100	4	3	Address 0
0x0101	5	2	Address 1
0x0102	6	1	Address 2
0x0103	7	5	Device Select
0x0104	9	4	Command Strobe
0x0105	10	8	Shift Clock
0x0106	11	6	Clock Data Input

The control inputs on U19 are set by the CPU through U18 so that a bit of data from the clock is present on U19 pin 9 which is input to the CPU via U17 pin 4 by a CRU input cycle that addresses this input.

U17 is also used to input data from the communication interface circuit blocks.

Clock frequency is controlled by Y2, a 32.768 kHz crystal. Capacitors C15 and C16 are required to maintain oscillator operation and stability. Resistor R31 is a pull-up resistor for the clock data output on U19 pin 9, since this output is open drain.

Host Communication Circuit

The host communication circuit provides the interface between the CPU and the serial, asynchronous, communication channel with the host computer. The line driver and receiver portion of the circuit can be switch selected to EIA voltage levels with RS-232-C protocol or RS-422 differential voltage levels.

Data exchange with the CPU is done with a TMS-9902A asynchronous communications controller (ACC), using the CRU interface hardware.

The ACC, U14, is enabled at pin 17 when the output of U22 pin 14 is asserted low, which will happen when the CPU is sending data to or receiving data from the ACC. The CPU sends control information and data to the ACC on a CRU output cycle. The CPU receives control information and data from the ACC on a CRU input cycle. The identification of each bit of data transferred is determined by addresses A1 through A5 with the state of the data for the ACC defined by address bit A0, and the state of the data for the CPU defined on pin 4 of the ACC.

The connection between the Front End and the host computer is made through connector J70. A six-position DIP switch, S1, is used to select between EIA RS-232-C and RS-422 communication types.

RS-232-C COMMUNICATION

When RS-232-C communication is used, the host sends characters to J70 pin 3. The EIA voltage-level signal is converted to TTL signal levels by U6, a quad line receiver, and passed to U14 pin 3. When the ACC detects that a character has been received, the CPU is notified with an interrupt and inputs the character from the ACC. The Clear to Send (CTS) and Data Set Ready (DSR) signals from the host computer are level shifted by U6 and passed to U14 on pins 7 and 6, respectively. When the ACC has a character to send to the host computer, the signal is output with the configuration switch-selected characteristics on pin 2 of U14, the ACC. This TTL-level signal is converted to EIA voltage levels by U5, a quad line driver, and passed to J70 pin 2 for reception by the host computer. The Request to Send (RTS) signal from U14 pin 5 is level shifted by U5 and passed to J70 pin 4. This communication will take place provided all of the RS-232-C control signals are asserted properly. If a "three wire connection" is used to the host, U6 is biased to interpret these open inputs as asserted and provides the appropriate control inputs to U14, the ACC. Capacitors C3, C7 and C8 along with resistors in resistor networks Z4 and Z5 provide noise filtering at U6.

RS-422 COMMUNICATION

When RS-422 communication is used, the host sends characters to J70 pins 14 and 15. The differential voltage input is converted to TTL signal levels by U3, a dual differential line receiver, and passed to U14 pin 3. The response of U14 from this point is the same as for RS-232-C. An output character from the ACC, is converted from TTL levels to a differential voltage level by U7, a dual differential line driver, and passed to J70 pins 9 and 10. Line drive is improved by using both drivers of U7 in parallel and resistively coupling their outputs with R16 through R19 to allow for a non-fatal driver failure. Resisters R20 and R21 provide current limit protection. Resistors R13 and R15 provide line termination for receive inputs. Resistors R12 and R14 provide a defined input for U3 when the inputs are left open.

Serial Link Communication Circuit

The serial link communication circuit provides the interface between the CPU and the RS-422 serial communication channel with its associated measurement and control options (referred to as serial link devices).

Data exchange with the CPU is done with a TMS-9902A asynchronous communications controller (ACC), using the CRU interface hardware.

The ACC, U11, is enabled at pin 17 when the output of U22 pin 13 is asserted low, which will happen when the CPU is sending data to or receiving data from the ACC. The CPU sends control information and data

to the ACC on a CRU output cycle. The CPU receives control information and data from the ACC on a CRU input cycle. The identification of each bit of data transferred is determined by addresses A1 through A5 with the state of the data for the ACC defined by address bit A0, and the state of the data for the CPU defined on pin 4 of the ACC.

The interconnection of the Computer Interface Assembly and serial link devices installed in the Front End is made through P12 (via the Motherboard PCA). The interconnection of the Computer Interface Assembly and serial link devices installed in Extender Chassis is made through J23 (via appropriate cabling).

A character for serial link output that has been transferred to U11, the ACC, is serially output by U11 on pin 2 and converted from TTL levels to RS-422 differential voltage levels by U1, a dual differential line driver. Line drive is improved by using both drivers of U1 in parallel and resistively coupling their outputs with R4 through R7 to allow for a non-fatal driver failure. CR4 through CR7 provide voltage protection for U1, and R2 and R3 provide current limit protection.

A character for input from a serial link device is converted from differential voltage levels to TTL-levels by U3, a dual differential line receiver, and passed to U11 pin 3. When U11 detects that a character has been received, the CPU is notified with an interrupt and inputs the character from the ACC. Resistors R8 through R11 provide line termination for the receive inputs. Diodes CR8 through CR11 provide voltage protection for U3.

Interrupt Control Logic

The serial link ACC is operating at 25,000 baud, so the interrupt on pin 1 is connected directly to the INT1(L) input of U20, pin 15.

The host computer ACC interrupt on pin 1 is low OR-ed by U9 with other possible ACC interrupts to produce a composite interrupt on U9 pin 12 that is connected to the INT4(L) input of U20, pin 14. Since U12 and U13 are for future expansion, R22 and R23 pull-up resistors are used to keep these interrupt lines from floating. The INT1(L) input on U20 has a higher priority than the INT4(L) input.

Power Distribution

Power is delivered to the Computer Interface Assembly from the mainframe power supply by an 8-conductor cable that connects at J75. TP1 through TP4 are provided to monitor the +5V, +12V, and -12V power sources at the Computer Interface Assembly. VR1, a 6V Zener diode, provides protection against voltage transients.

When Front End power is ON, and W9 (the battery power disconnect jumper) connects the negative terminal of the battery to ground, the +5V supply provides +5B through CR1 and charges BT1 through R1 and CR3. When Front End power is OFF, the battery (BT1), supplies +5B through CR2.

POWER SUPPLY

The power supply is a switch mode supply that operates at either 90 to 132V ac or 180 to 264V ac (depending on a jumper setting), at a frequency range between 47 through 440 Hz.

The ac line voltage is transformed to regulated +5V, +12V and -12V dc voltages. The power supply connector pinouts are shown in Table 3-5.

Table 3-5. Power Supply Connector Pinouts

J1 (INPUT)		J2, J3, & J4 (OUTPUT)	
PIN	**SIGNAL**	**PIN**	**SIGNAL**
1	AC Neutral	1	-12V
2	AC Line	2	+12V
E3	AC Ground	3	Return
		4	+5V

See Section 7 of this manual for a schematic diagram of the power supply.

SERIAL LINK COMMUNICATION

Hardware

The serial link connects the Computer Interface Assembly with data acquisition and control options in the system.

NOTE

In this discussion, the data acquisition and control options are collectively called "devices."

The serial link controller (i.e., Computer Interface Assembly) translates TTL-level signals from the CPU into RS-422 signals for communication with the devices. The RS-422 signals are sent and received over two twisted pairs of conductors. On one pair, the controller transmits while all devices listen. On the other pair, a device selected by the controller can transmit responses to the controller, but never to other devices.

Devices on the serial link may be physically located inside the Front End or in an Extender Chassis. The serial link is routed through each device in such a way that if power is removed from any of them, communication through the link remains unbroken.

General Protocol

This description deals only with the elements of the serial link protocol that are device independent. Because of the diversity of devices, only the most basic protocol can be covered.

Information is sent over the serial link in the form of ASCII characters at a rate of 25000 baud. Each character consists of the following:

1 Start Bit
8 Information Bits
1 Odd Parity Bit
1 Stop Bit

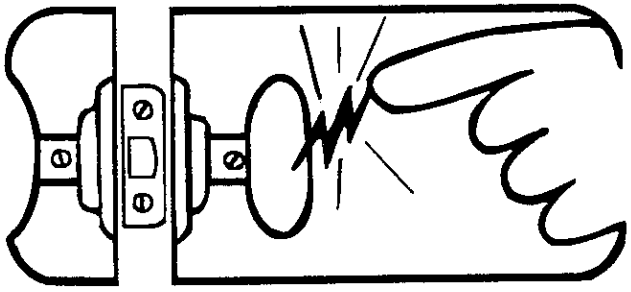
When the controller sends a message, the addressed device replies with either an acknowledgement or a response message (depending on the message type). A device never initiates an exchange.

A message is sent in one or more groups. The group is the basic protocol unit and consists of three information characters followed by a check character. Some controller messages require the device to reply with an acknowledgement, which is a single character and can have one of only two values: ready (0x3C), and not ready (0xC3).

The serial link is protected against occasional errors in transmission by character parity and longitudinal parity. The protocol recovers by repeating the transmission.

static awareness

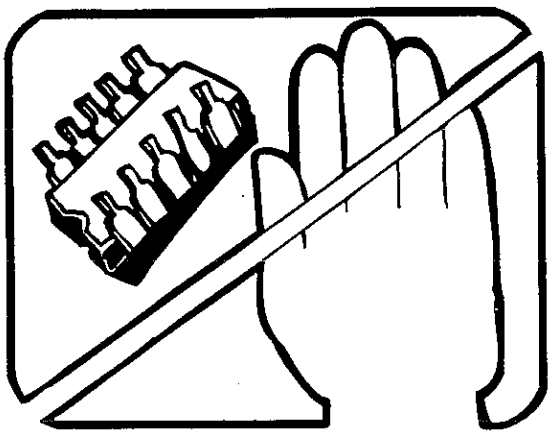
A Message From
Fluke Corporation



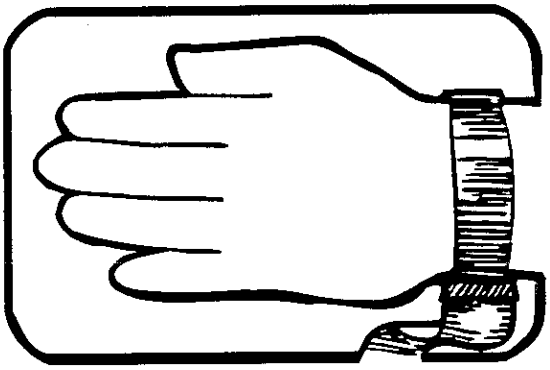
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Leaning the guidelines for handling them.
3. Using the procedures, packaging, and bench techniques that are recommended.

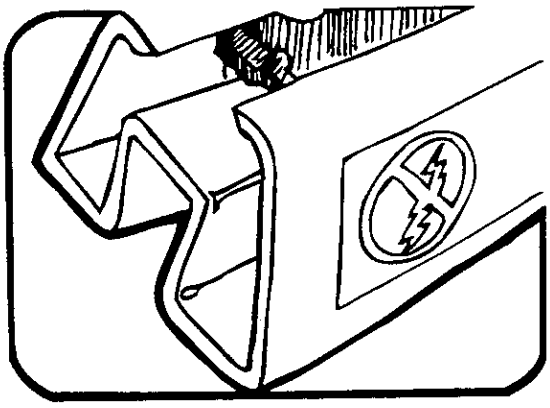
The following practices should be followed to minimize damage to S.S. (static sensitive) devices.



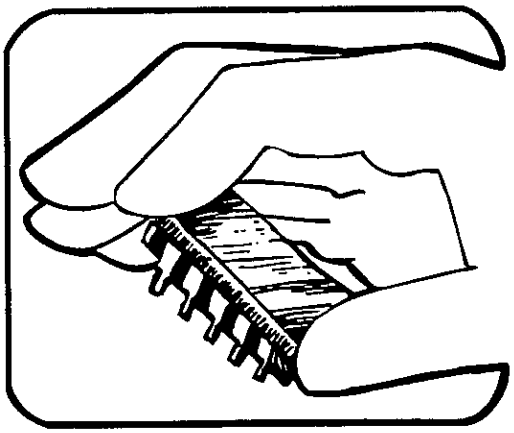
1. MINIMIZE HANDLING



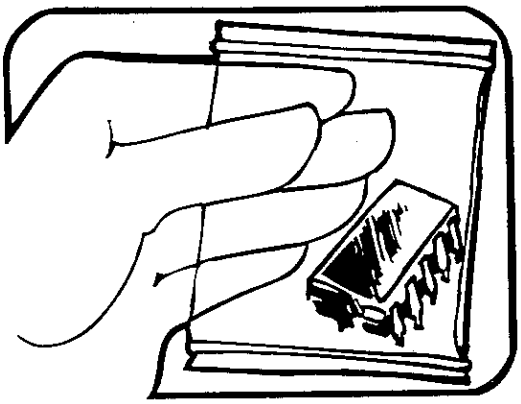
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



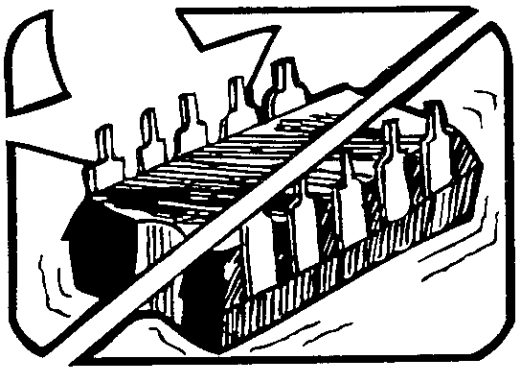
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



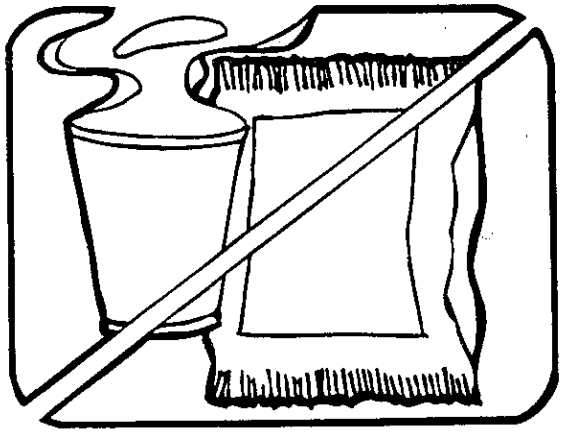
4. HANDLE S.S. DEVICES BY THE BODY.



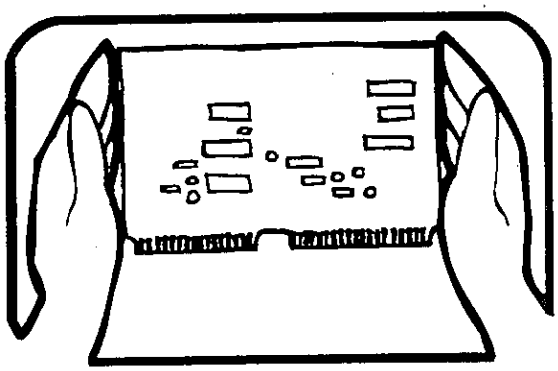
5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT.



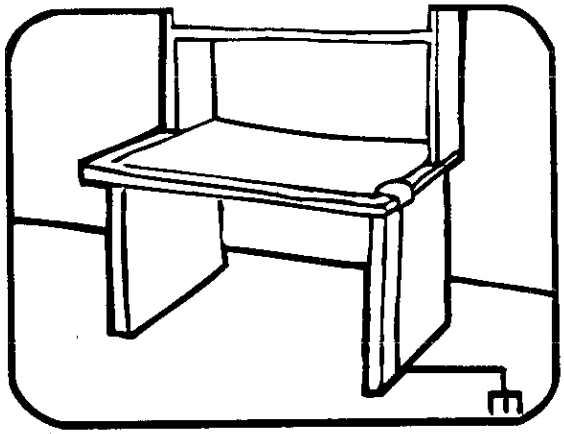
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE.



7. AVOID PLASTIC,VINYL AND STYROFOAM® IN WORK AREA.



8. WHEN REMOVING PLUG-IN ASSEMBLIES HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS PROTECT INSTALLED S.S. DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION.

10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

11. ONLY GROUNDED-TIP SOLDERING IRONS SHOULD BE USED.

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SECTION 4
MAINTENANCE

CONTENTS

INTRODUCTION

Section 4 contains procedures for performing general maintenance on and accessing and cleaning all major assemblies of the Front End mainframe.

NOTE

If the Front End is equipped with a Scan/Alarm option (-201), a different Computer Interface Assembly is used. Related maintenance instructions are found in Section 9A of this manual.

GENERAL MAINTENANCE

Line Voltage Selection

Refer to Section 9A for Scan/Alarm Option -201 line voltage selection instructions.

WARNING

THE FOLLOWING PROCEDURE REQUIRES ACCESS TO THE INTERIOR OF THE COMPUTER FRONT END. DO NOT PERFORM THIS PROCEDURE UNLESS YOU ARE QUALIFIED TO DO SO. LETHAL VOLTAGES MAY EXIST WITHIN THE UNIT.

The power input setting (110V or 220V) is normally marked on the support panel of the Computer Interface Module, just above the power input connector. If there is no mark in either box, or if the box is marked for a voltage other than the one you will be using, use the following procedure to gain access to the internal setting.

1. Turn the Computer Front End power switch to OFF.

2. Remove the ac input line cord from the power source and from the Computer Front End.

3. Remove the four Phillips-head screws indicated in Figure 4-1.

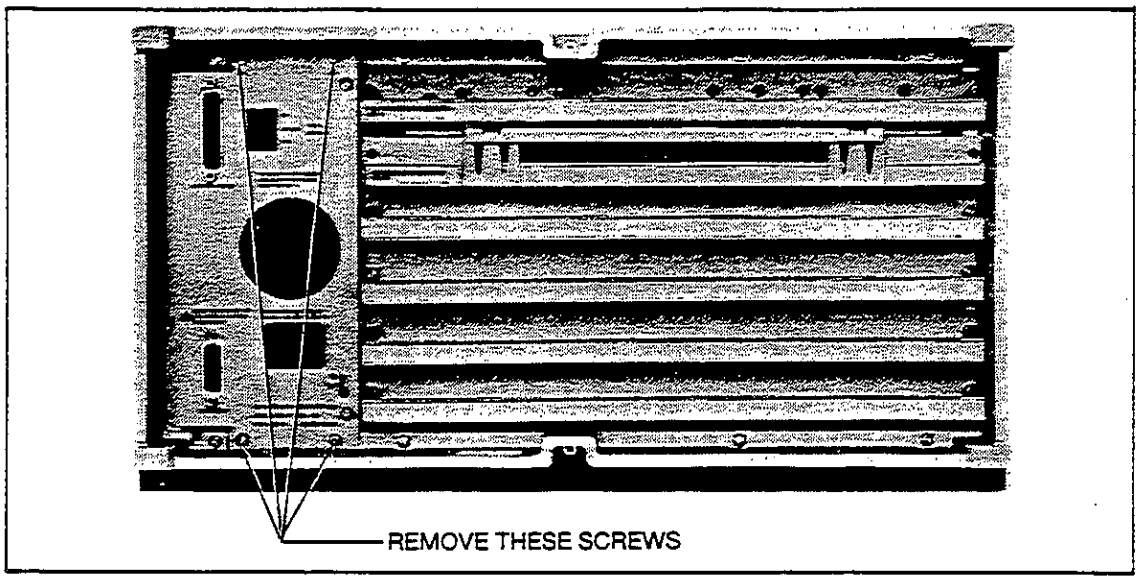

Figure 4-1. Computer Interface Module Supply Removal Screws

4. Remove the Computer Interface Module from the chassis by grasping the finger indentation in the fan filter hole (as shown in Figure 4-2) and sliding the module straight back and out.

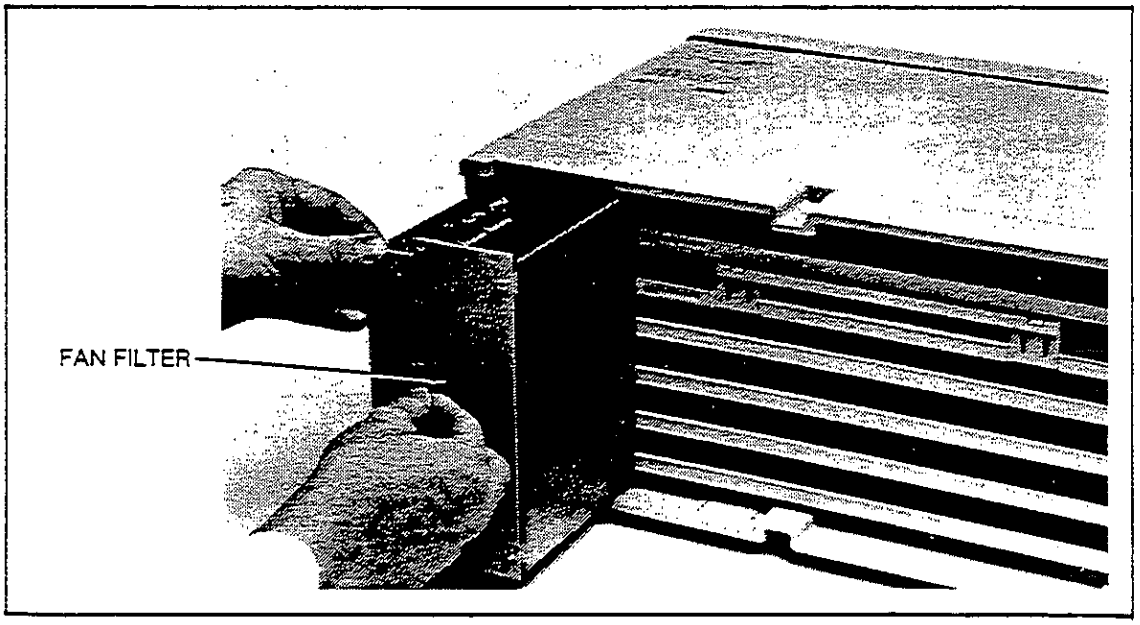

Figure 4-2. Removing the Computer Interface Module

5. Refer to Figure 4-3 to locate the Line Power Voltage Pins on the Power Supply PCA.

   To select 180-264V operation, connect the wire to the pin marked 220V. For 90-132 operation, place the wire on the pin labeled 110V.

NOTE

It is not necessary to change the power input fuse when changing the power supply operating voltage.

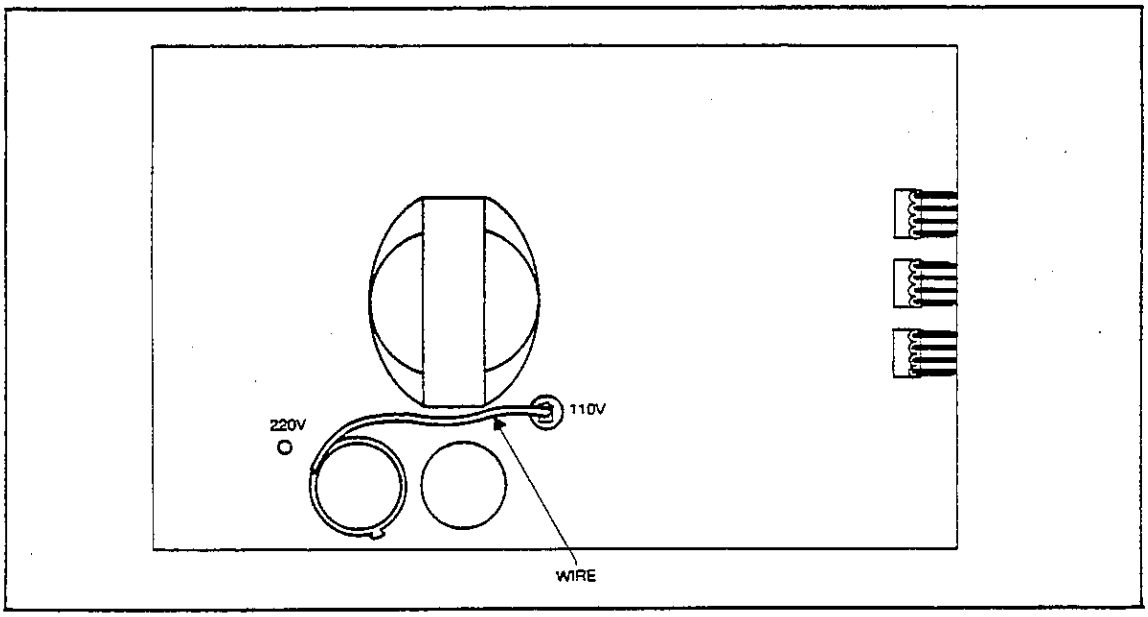

Figure 4-3. Line Power Voltage Pins

6. While the Computer Interface Module is out, locate the Line Frequency Selection Switch, S3-8, (see Figure 4-4) to ensure that it is set to the local line frequency.

   If the switch is not set to the local line frequency, set it properly before continuing. For 50-Hz operation, place S3-8 in the 0 position (toward the card edge). For 60-Hz operation, place the switch in the 1 position.

7. After changing the line power voltage, mark the appropriate power setting on the support panel of the module, (above the ac input socket where the words "WIRED FOR" are embossed).

8. Slide the Computer Interface Module back into the Front End, and reinstall the Phillips-head screws.

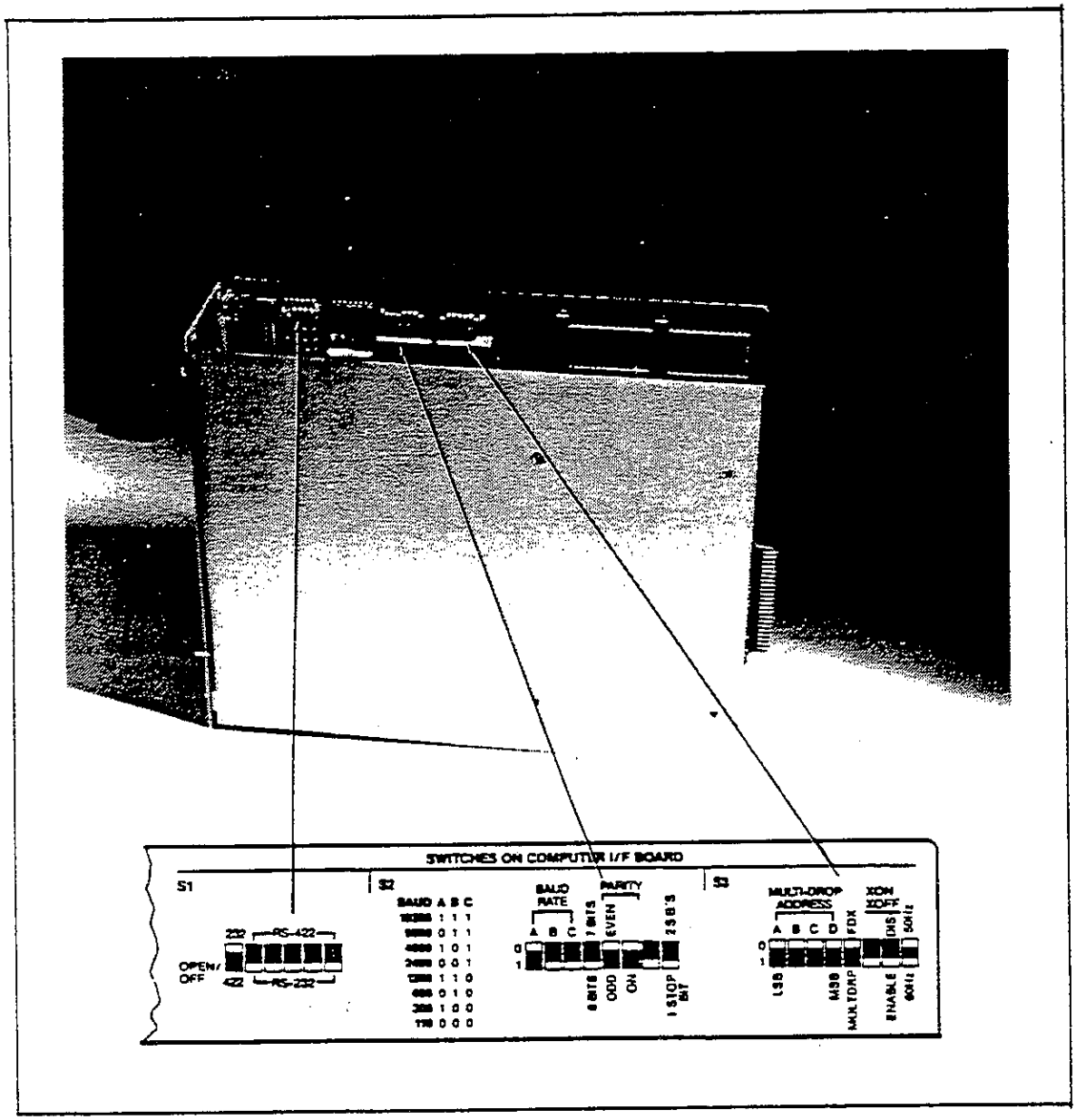

Figure 4-4. Communication Parameter Selection Switches

Fuse Replacement

The fuse is located on a clip-type holder on the power supply assembly, in the corner to the right of the 110V voltage selection pin. When replacing the fuse, use the same value (2.0A, 250V). To check or replace the fuse, perform the following:

1. Switch OFF power to the Front End and disconnect the ac line cord and other high voltage input.

2. Remove the Computer Interface Module as described in steps 3 and 4 of the Line Voltage Selection procedure (above).

3. Use a slotted screwdriver or adjustment tool to remove the fuse.

4. After checking or replacing the fuse, reinstall the Computer Interface Module in the Front End chassis and test its operation.

Power Supply Adjustments

The power supply voltage levels do not normally require calibration, although some minor service adjustments may occasionally be necessary. Refer to Section 5 for power supply adjustment procedures.

General Cleaning

CAUTION

Before cleaning or servicing the Computer Interface Assembly, disconnect back-up battery power by moving the W9 jumper as shown in Figure 4-5.

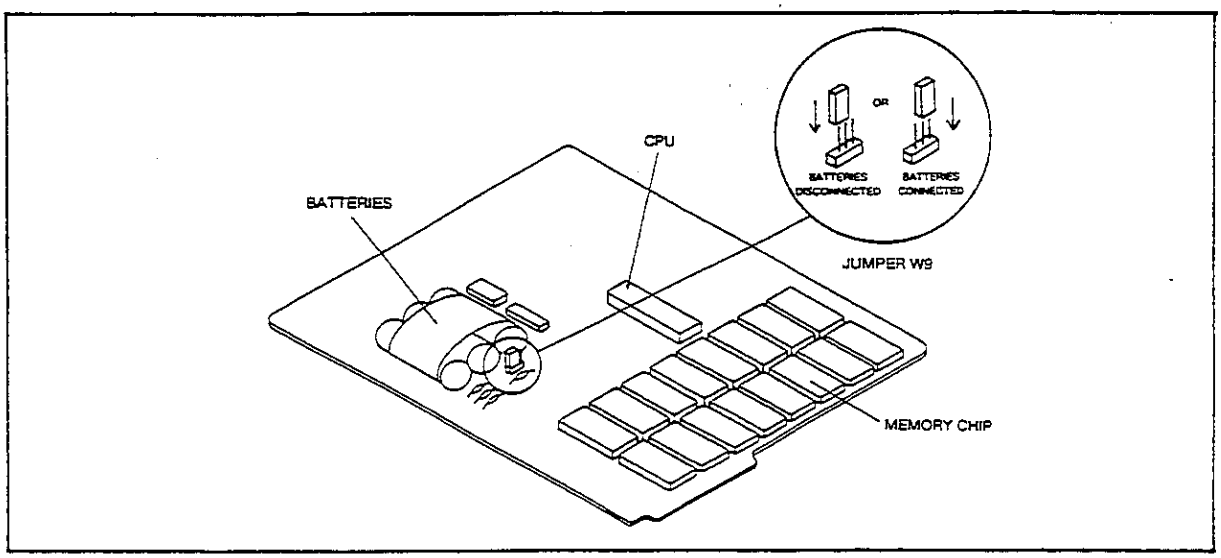

Figure 4-5. W9 Battery Power Jumper

CAUTION

Do not use aromatic hydrocarbons (such as naphthalene) or chlorinated solvents (such as carbon tetrachloride) for cleaning. They may damage plastic materials used in the instrument.

Wipe the Computer Front End periodically to remove dust, grease, and other contamination. The Front End chassis may be wiped using a soft cloth dampened with a mild solution of detergent and water. Dry the case thoroughly after cleaning.

Do not apply fluids or detergents directly to the chassis.

Observe the following precautions when cleaning the Front End:

- Handle a pca by its edges rather than by its connector pins.

  Oils from your skin can contaminate the board and degrade measurement accuracy of the system.

- Improper handling can also cause instantaneous or delayed electrostatic discharge damage.

  The yellow "Static Awareness" sheet preceding this section explains some of the hazards of static electricity to sensitive components.

- Do not use a static-inducing vacuum brush to clean assemblies. Possible electrostatic discharge can damage sensitive components.

PCA Cleaning

Unless dirt, dust or other contamination is visible on its surface, a pca does not normally require cleaning.

When significant dirt or contamination is visible, clean the board(s) with low pressure air (less than 20 psi). If air cleaning is not possible, clean the board with water-based cleaning equipment.

If commercial water-based cleaning equipment is not available, clean the board by holding it under warm, running water.

The Motherboard may be cleaned by removing it (as explained in Section 4, below) and using a FREON degreaser or warm water. Thoroughly dry the Motherboard (use only forced air, not heat) before reassembly.

Observe the following precautions when using water-based cleaning equipment:

1. Read and observe all precautions listed previously under General Cleaning.

2. Remove all board shielding covers, and separate any relay piggy-back assemblies.

3. In areas with exceptionally hard water, use either deionized or distilled water for a final wash to remove ions left by the hard water wash.

4. Dry all boards thoroughly. Use a low-temperature drying chamber or an infrared drying rack with a temperature range between 100 and 120 ^{o}F (38 to 46 ^{o}C) if available.

5. If a drying chamber or infrared drying rack is not available, air dry the board at room temperature for a minimum of 48 hours before reassembling.

6. Use a mixture of 70% isopropyl alcohol and 30% water and a lint-free cloth to clean edge-connector contacts. Never use an eraser to clean connector contacts; it might generate static or abrade the gold plating on the contacts.

Fan Filter Cleaning

Clean the fan filter (shown in Figure 4-2) any time it is visibly contaminated. If the Front End is operated too long with a dirty air filter, heat buildup inside could damage sensitive electronic components.

To clean the filter, pinch the center and pull directly out. Clean the filter with warm soapy water and rinse it thoroughly before replacing.

ACCESS, REMOVAL AND REINSTALLATION PROCEDURES

The following procedures provide step-by-step instructions for gaining access to, removing, and reinstalling major assemblies of the Computer Front End Mainframe. Refer to Figure 6-1 for the location of the major assemblies on the Front End chassis.

WARNING

THE FRONT END CONTAINS HIGH VOLTAGES THAT CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE FRONT END AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE FOLLOWING ACCESS PROCEDURES.

Access to Options

Front End module and connector options are accessible from the rear of the instrument.

An option board or connector may be removed by loosening the two retaining screws, one on each side, and sliding out the pca.

Removing and Reinstalling the Top and/or Bottom Cover

Use the following procedure to remove the top and/or bottom cover:

1. Disconnect all power cables and remove any connectors from the serial link options.

2. Remove the carrying straps from the sides of the instrument by removing the two Phillips-head screws at the ends of the handles.

3. Remove the three Phillips-head screws located in the handle indent groove of the cover on each side of the Front End.

4. From the rear of the Front End, remove the top or bottom counter-sunk Phillips-head screw located in the top recess of the rear bezel, and remove the desired cover.

Reverse the previous steps to reinstall the top and/or bottom cover(s).

Removing and Reinstalling the Front Panel

Use the following procedure to remove the front panel from the Front End:

1. Disconnect all power to the Front End.

2. Remove the decals bearing the name Fluke from the sides of the instrument.

3. Remove the three exposed screws from each side of the unit. If the 2289A was rack mounted, remove the rack ears from the side of the instrument and reemove the screws underneath.

4. Pull off the plastic front bezel.

5. Pry off the front panel being careful not to overextend the wire connected to the front panel LED.

6. Desolder LED red and white wires from motherboard noting their locations for reinstallation.

7. From behind the front panel, gently push the LED forward and out.

8. Reinstall the LED before installing the front panel. Push the LED through the hole on the front panel and solder its wires to the motherboard as noted in step #6.

Reverse the previous steps to reinstall the front panel.

Removing and Reinstalling the Motherboard

Use the following procedure to remove the Motherboard from the Front End chassis.

1. Remove the top and bottom covers as described under Removing and Reinstalling the Top and/or Bottom Cover (above).

2. Remove the front panel as described under Removing and Reinstalling the Front Panel (above).

3. Carefully remove the brass gasket from the rear of the unit.

4. Remove the six Phillips-head screws along the outside edge of the unit, and remove the top part of the chassis.

5. Remove the black serial link device card guide.

6. Slide the Motherboard out towards the top of the instrument.

Reverse the previous steps when reinstalling the Motherboard.

To ensure that the Motherboard is reinstalled properly, without damaging it or the Front end chassis, remember to:

- Reinstall the Motherboard with the P12 connector in the lower left corner as you face the Front End from the rear.

- Reinstall the device guide with its Motherboard locating peg in the corresponding hole.

- Reinstall the LED before installing the front panel.

Removing and Reinstalling the Power Supply

Refer to Section 9A for Scan/Alarm Option -201 power supply removal and installation instructions.

WARNING

THERE ARE LETHAL VOLTAGES AT VARIOUS POINTS ON THE POWER SUPPLY. EXERCISE EXTREME CAUTION WHEN SERVICING. DISCONNECT THE FRONT END FROM LINE POWER AND DISCHARGE ALL CAPACITORS AS SOON AS THEY ARE ACCESSIBLE.

The Power Supply PCA is mounted on the Computer Interface Module (Figure 4-6).

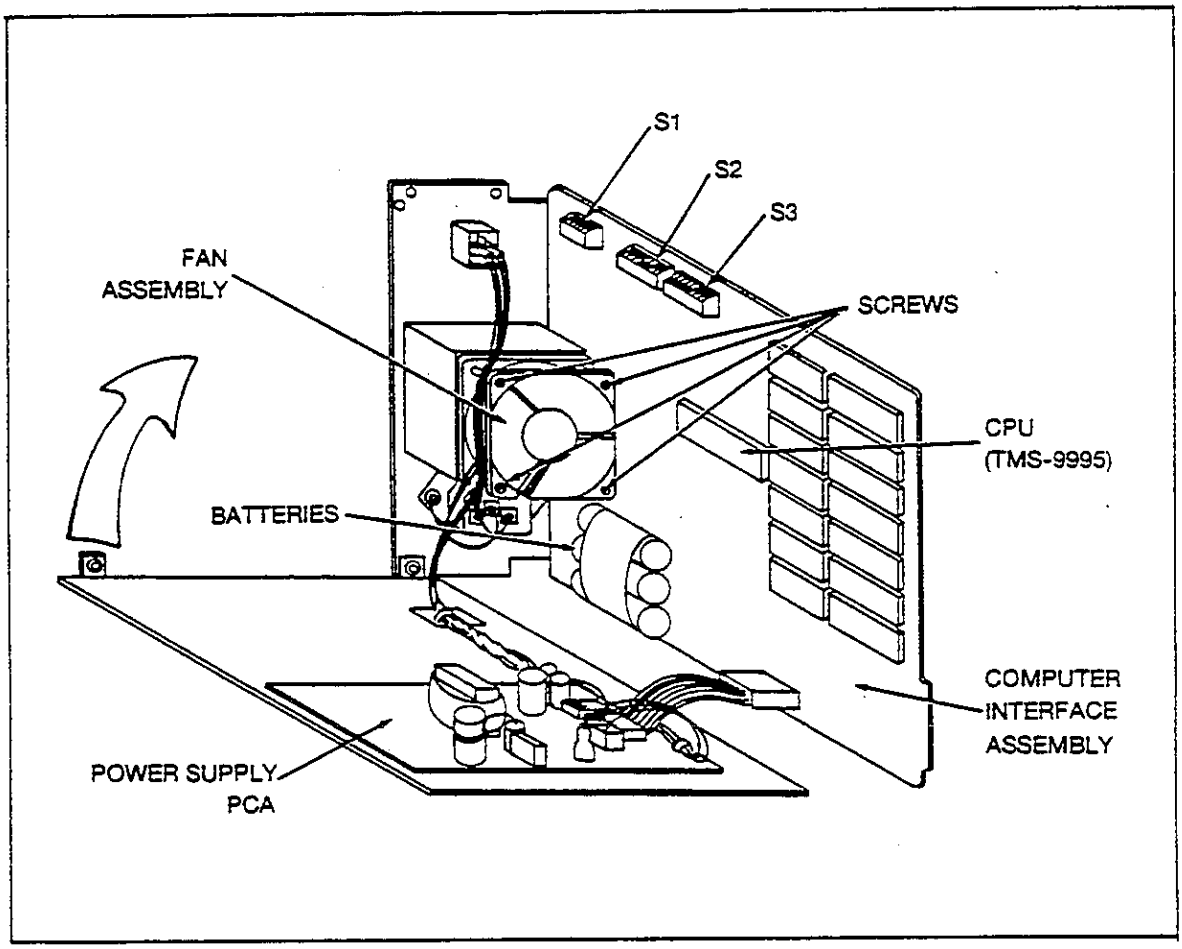

Figure 4-6. Computer Interface Module (Interior)

To access the Power Supply PCA, use the following procedure:

1. Switch OFF power to the Front End and disconnect the ac line cord from the support panel input connector.

2. Remove the four Phillips-head screws (shown in Figure 4-1) that secure the Computer Interface Module to the mainframe chassis.

3. Remove the Computer Interface Module from the chassis by grasping the finger indentation in the fan filter hole (as shown in Figure 4-2) and sliding the module straight back and out.

4. The Power Supply PCA is secured to the right panel of the Computer Interface Module by four Phillips-head screws. To access these screws, first disconnect the right panel from the Computer Interface Module support panel by removing the two securing nuts.

5. Disconnect all leads connecting the power supply to the Computer Interface Assembly, power switch and fan assembly.

6. To detach the power supply from the right panel, remove four Phillips-head screws, one in each corner of the power supply.

Reverse the previous steps to reinstall the Power Supply.

Removing and Reinstalling the Computer Interface Assembly

Refer to Section 9A for Scan/Alarm Option -201 Computer Interface Assembly removal and installation instructions.

CAUTION

Handle the Computer Interface Assembly with care, or some semiconductors and ICs can be damaged by electrostatic discharge during handling. Refer to the static awareness information at the beginning of this section for proper handling precautions.

The Computer Interface Assembly is mounted on the Computer Interface Module (see Figure 4-6). Use the following procedure to access the Computer Interface Assembly:

1. Perform steps 1 through 3 of the Removing and Reinstalling the Power Supply procedure (given earlier in Section 4).

2. Disconnect all leads from the power supply to the Computer Interface Assembly.

3. Place jumper W9, shown in Figure 4-5, in the "batteries disconnected" position.

4. The Computer Interface Assembly is secured to the left panel of the Computer Interface Module by four hex-head screws above and below the host computer and extender chassis connectors.

   Remove the hex-head screws to detach the Computer Interface Assembly from the side panel.

NOTE

The Computer Interface Assembly should be stored and transported in an anti-static bag.

Reinstall the Computer Interface Assembly by reversing these steps.

Removing and Reinstalling the Fan Assembly

Refer to Section 9A for Scan/Alarm Option -201 fan assembly removal and installation instructions. To remove the fan assembly attached to the standard Computer Interface Assembly, (shown in Figure 4-6), perform the following procedure:

1. Perform steps 1 through 4 of the Removing and Reinstalling the Power Supply procedure (given earlier in Section 4).

2. Disconnect the red and blue leads between the power supply and fan assembly if this has not already been done.

3. To detach the fan assembly (and the fan filter housing) from the front panel of the Computer Interface Module, remove the four screws (shown in Figure 4-6) which secure the fan assembly and filter housing to the panel.

To reinstall the fan assembly reverse the previous steps.

SECTION 5
TESTING AND TROUBLESHOOTING

CONTENTS

INTRODUCTION

Section 5 contains performance testing and troubleshooting information for the Helios I Computer Front End mainframe. Performance testing of Front End options is covered in Section 8 (Options -160 through -169), Section 9 (Options -170 through -179), and Section 9A (Option -201).

Mainframe performance testing consists of two procedures: the Mainframe Test and the System Selftest. These tests, which can also serve as initial acceptance tests, verify correct operation of the interface (RS-232-C/RS-422) and interface hardware (ROM, RAM, UART).

The troubleshooting procedures assist service personnel in tracing a malfunction to the printed circuit assembly (pca) level. If a defective pca is identified, we recommend that repair be accomplished using the Fluke Module Exchange Program. For additional information, refer to the Introduction in Section 1.

The mainframe theory of operation (Section 3) and schematics (Section 7) can be used by qualified personnel to troubleshoot the Front End circuit assemblies to the component level. Before troubleshooting to the component level, however, it is advisable to contact a Fluke Service Representative.

PERFORMANCE TESTING

WARNING

THE COMPUTER FRONT END CONTAINS HIGH VOLTAGES THAT CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE INSTRUMENT. TURN OFF THE COMPUTER FRONT END AND REMOVE ALL POWER SOURCES BEFORE PERFORMING THE FOLLOWING PROCEDURES.

Mainframe Testing

To verify that the Front End mainframe has been correctly installed and is operating properly, perform the following:

1. Switch OFF power to the Front End. Disconnect the ac line power cord and all other high voltage inputs.

2. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, number of data bits, number of stop bits) on the Front End and the host (terminal or computer) are properly configured to send and receive serial data.

   This is done by following the instructions under the heading "Setting the Communication Switches" in Section 3A of the Helios I System Manual). If the Computer Interface Assembly was removed to check (or set) the communication parameters, reinstall it at this time.

3. Remove all installed options from the Front End.

4. Directly connect the host (computer or terminal) to the Front End using equipment and cables appropriate to the type of electrical interface (RS-232-C or RS-422).

   Check to make sure connections are tight.

5. Reconnect the ac line cord to the Front End and switch the power ON.

6. Switch ON power to the host.

7. Program the Front End using either a terminal or a computer. (You can also run a terminal emulation program to use a computer behaving as a terminal.) For ease of testing, a terminal is the recommended host.

   Use either PROCEDURE A or PROCEDURE B, depending on whether performance testing will be done in Terminal or Computer Mode.

PROCEDURE A. TERMINAL MODE

If a terminal or a computer emulating a terminal is the selected host, send the following commands to the Front End.

MODE=TERM <CR>

SEND VERSION$ <CR>

The response from the Front End to the host should be:

Helios-I Version x.y

or

Helios Scan/Alarm Version x.y Software by Polar Software Systems

Where x.y is the version number of the installed firmware.

If this response is not returned, a malfunction has occurred.

If "Helios Scan/Alarm Version x.y Software by Polar Software Systems" is returned, perform the additional Alarm Annunciator and Printer Output tests presented in Section 9A.

PROCEDURE B. COMPUTER MODE

The following sample BASIC programs cause the Front End to respond with its installed version number. One program was written for an IBM* PC and one for a Fluke 1722A Instrument Controller. These programs assume that the Front End has been configured for 9600 baud, no parity, 8 data bits, and 1 stop bit.

---

* IBM is a trademark of International Business Machines Corporation.

NOTE

These programs are examples. If you do not have an IBM PC or a Fluke 1722A Instrument Controller, enter a program that will run on your host.

Program for IBM PC:

```
10   CLOSE 1
20   CLS
30   REM open communication port, empty Front End buffer
40   OPEN "com1:9600,n,8,1,cs,ds,cd" AS #1
50   PRINT #1,CHR$(3);
60   REM set up Front End
70   PRINT #1,"mode=comp"
80   GOSUB 300
90   REM request message and read in response
100  PRINT #1,"send version$"
110  LINE INPUT #1,M$
120  PRINT M$
130  END
300  REM wait for message accepted prompt
310  INPUT #1,A$
320  IF A$<>"!" THEN GOTO 310
330  RETURN
```

Program for 1722A:

```
10   CLOSE 1,2
20   PRINT CHR$(27);"[2J";
30   REM open communication port and empty Front End buffer
40   OPEN "KB1:"AS NEW FILE 1%
50   OPEN "KB1:"AS OLD FILE 2%
60   PRINT #1,CHR$(3);
70   REM set up Computer Front End
80   PRINT #1,"mode=comp"
90   GOSUB 300
100  REM request message and read in response
110  PRINT #1,"send version$"
120  INPUT #2,M$
130  PRINT M$
140  END
300  REM wait for message accepted prompt
310  INPUT #2,A$
320  IF A$<>"!" THEN GOTO 310
330  RETURN
```

The response from the Front End to the host should be:

Helios-I Version x.y

or

Helios Scan/Alarm Version x.y Software by Polar Software Systems

Where x.y is the version number of the installed firmware. If this response is not returned, a malfunction has occurred.

If "Helios Scan/Alarm Version x.y Software by Polar Software Systems" is returned, perform the additional Alarm Annunciator and Printer Output tests presented in Section 9A.

8. This completes the Mainframe Test.

If the Front End has failed this test, check all connections, then perform the test again. If the system fails the test a second time, determine if the interface of the host is functioning properly by testing it with another system or device. If the host interface is not at fault, contact your nearest Fluke Service Representative (see Appendix B).

System SelfTest

The system wide selftest determines if the read only memory (ROM), random-access memory (RAM), and the serial link universal asynchronous receiver-transmitter (UART) are operating properly.

1. Perform the Mainframe Test immediately preceding the System Selftest.

2. Perform a system selftest using PROCEDURE A (Terminal Mode) or PROCEDURE B (Computer Mode).

PROCEDURE A. TERMINAL MODE

If Terminal Mode is being used, send the following command to the Front End:

```
MODE=TERM <CR>
TEST <CR>
```

If a malfunction is detected, an error message will be returned.

If the Front End passes the selftest routine, the normal Terminal Mode prompt

```
HCLI>
```

is returned.

PROCEDURE B. COMPUTER MODE

If Computer Mode is being used, modify the program entered in PROCEDURE B of the Mainframe Test (above) to send the TEST command to the Front End and read its response. Make this modification by changing line 100 of the IBM program or line 110 of the 1722A program to:

```
PRINT #1,"test"
```

3. Run the modified program.

   If a malfunction is detected, the test failure will be reported in the format:

   ?<error code>

   The number, <error code>, will be one of three numbers shown in the table below, which corresponds to one of the messages returned in the Terminal Mode.

ERROR CODE	ERROR MESSAGE	FAULT CONDITION
?20	?ROM failed	First priority failure. A bad ROM or faulty ROM control circuit was detected.
?21	?RAM failed	Second priority failure. A bad RAM or faulty RAM control circuit was detected.
?22	?SL UART failed	Third priority failure. A problem with the serial link UART was detected.

   If more than one failure is detected, only the error code or message for the highest priority failure is returned.

NOTE

The Computer Front End will operate after a selftest error has been reported. However, measurements may be unreliable.

4. The System Selftest is complete.

TROUBLESHOOTING

System Troubleshooting

Troubleshooting a Computer Front End system requires a general understanding of how a system operates. Before troubleshooting, review the system-level block diagram (in Figure 3-1) and the system theory of operation (in Section 3) to familiarize yourself with the interrelationship of the various assemblies that make a Helios I Computer Front End system.

The mainframe theory of operation (Section 3) and schematics (Section 7) can be used by qualified personnel to troubleshoot the Front End pcas to the component level. Before troubleshooting to the component level, however, it is advisable to contact a Fluke Service Representative.

Figure 5-1 provides a system troubleshooting tree. This tree will aid you in troubleshooting a Front End system to the assembly level by isolating a specific, malfunctioning assembly.

Keep the following considerations in mind when using the troubleshooting tree:

- It is assumed that Helios-to-host communication parameters have been properly set and that external interconnections between them have been properly established.

  Therefore, before starting to troubleshoot, ensure that the communication parameters (i.e., baud rate, number of bits, parity etc.) on the Front End and host are properly configured to send and receive serial data, and that the host transmit and receive signals are connected to the proper pins on the host connecter, J70, of the Front End.

- The troubleshooting tree covers only the most common sources of system malfunction. It does not cover all possible problems that may occur.

- The troubleshooting tree isolates only the assembly that is most likely the source of the problem. Other problem sources may exist.

- The troubleshooting tree can be used with any Front End system configuration and combination of options. Skip over blocks that are not pertinent to your system.

Power Supply Troubleshooting

WARNING

THERE ARE LETHAL VOLTAGES AT VARIOUS POINTS ON THE POWER SUPPLY. EXERCISE EXTREME CAUTION WHEN SERVICING. DISCONNECT THE FRONT END FROM LINE POWER AND DISCHARGE ALL CAPACITORS AS SOON AS THEY ARE ACCESSIBLE.

CAUTION

Running the power supply without a load may damage the power supply. While servicing the power supply, a 0.5A load on 5V should be provided.

Begin troubleshooting the power supply by checking the 250V 2A fast-blow fuse. In most cases, if the fuse is blown, the power supply should be replaced. In rare instances, replacing the fuse will correct the problem.

If the fuse is good, but problems traceable to the power supply are evident, minor adjustments to the power supply may be required. Use the following procedure to adjust the power supply.

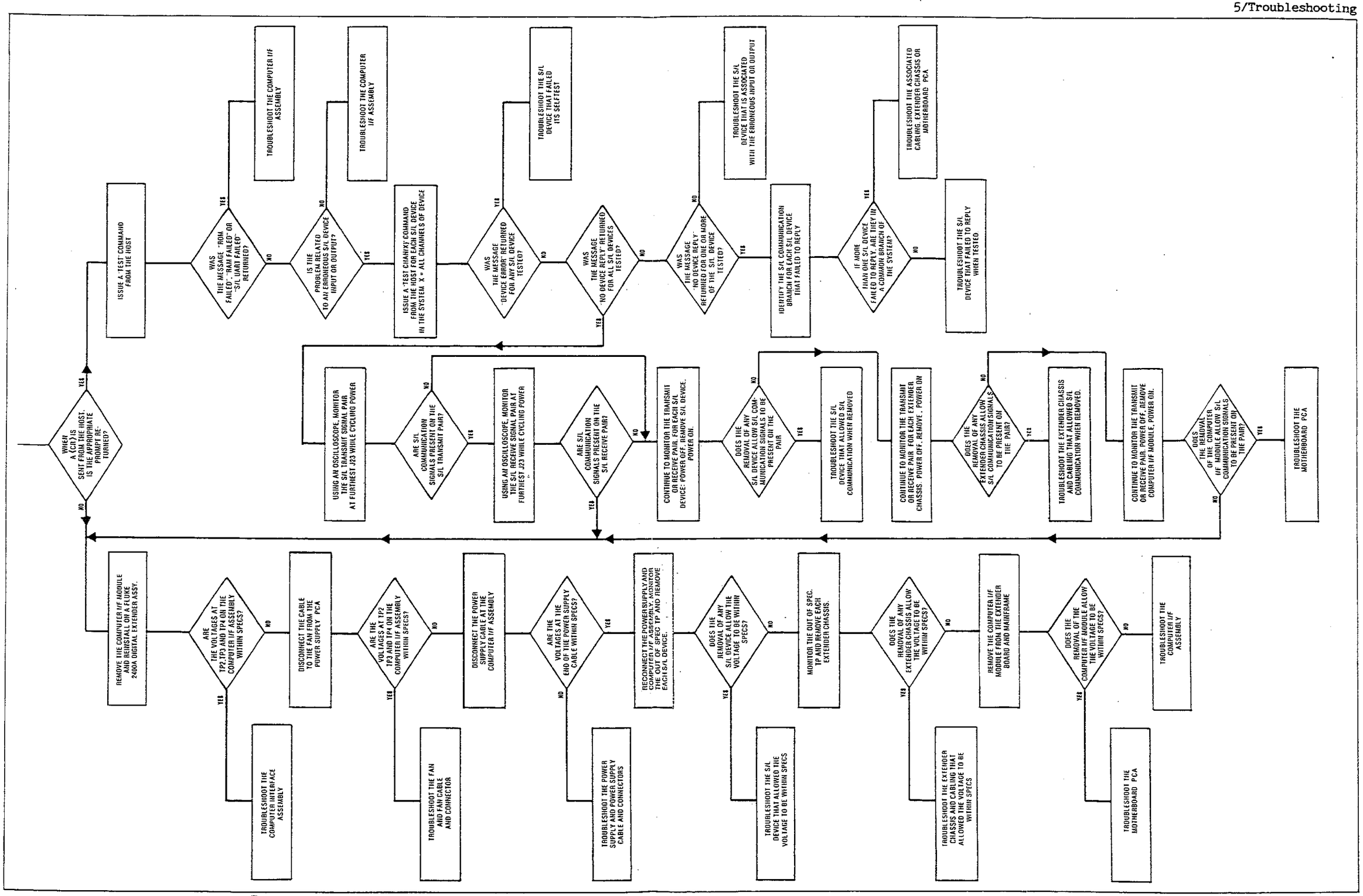

Figure 5-1. System Troubleshooting Tree

POWER SUPPLY ADJUSTMENTS

WARNING

CERTAIN COMPONENTS ON THE POWER SUPPLY HAVE BEEN SELECTED FOR ELECTRICAL CHARACTERISTICS NOT SPECIFIED ON THE COMPONENT. THEREFORE, THE POWER SUPPLY MAY FAIL EVEN IF THESE COMPONENTS ARE REPLACED WITH COMPONENTS OF THE SAME VALUE AND TOLERANCES. CONTACT THE POWER SUPPLY MANUFACTURER FOR THE PROPER COMPONENTS.

NOTE

Use a plastic screwdriver to adjust the power supply. A metal non-insulated screwdriver may cause a short if it comes in contact with metal on the chassis. After adjustment, a penetrating adhesive, such as Loctite*, should be used to hold the potentiometer in position.

Make service adjustments to the power supply as follows:

1. Use a DMM to measure the output from the power supply with respect to ground.

   If measuring at the power supply, see Table 3-5 for pin locations.

   If measuring at the Computer Interface Assembly see the schematic in Section 7 of this manual to locate the test points (TPs).

2. Probe the 5V pin.

   If the output is not within the specified 5.0V to 5.1V range, adjust the potentiometer to 5.1V, or adjust for 5.05V at TP4 on the Computer Interface Assembly.

3. Probe the +12V and -12V pins.

   If the 5V pin is within specifications, but the 12V pin is not within +/-5%, and the -12V pin is not within +/-10% (or the minor adjustments do not achieve the desired results), replace the power supply or suspect a short circuit in Front End or its option assemblies.

   Refer to "Power Supply Access" for instructions on removing and installing the power supply.

If it is necessary to troubleshoot the power supply to component level, refer to the power supply schematic in Section 7.

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* Loctite is a registered trademark of the Loctite Corporation.